FIG. 1

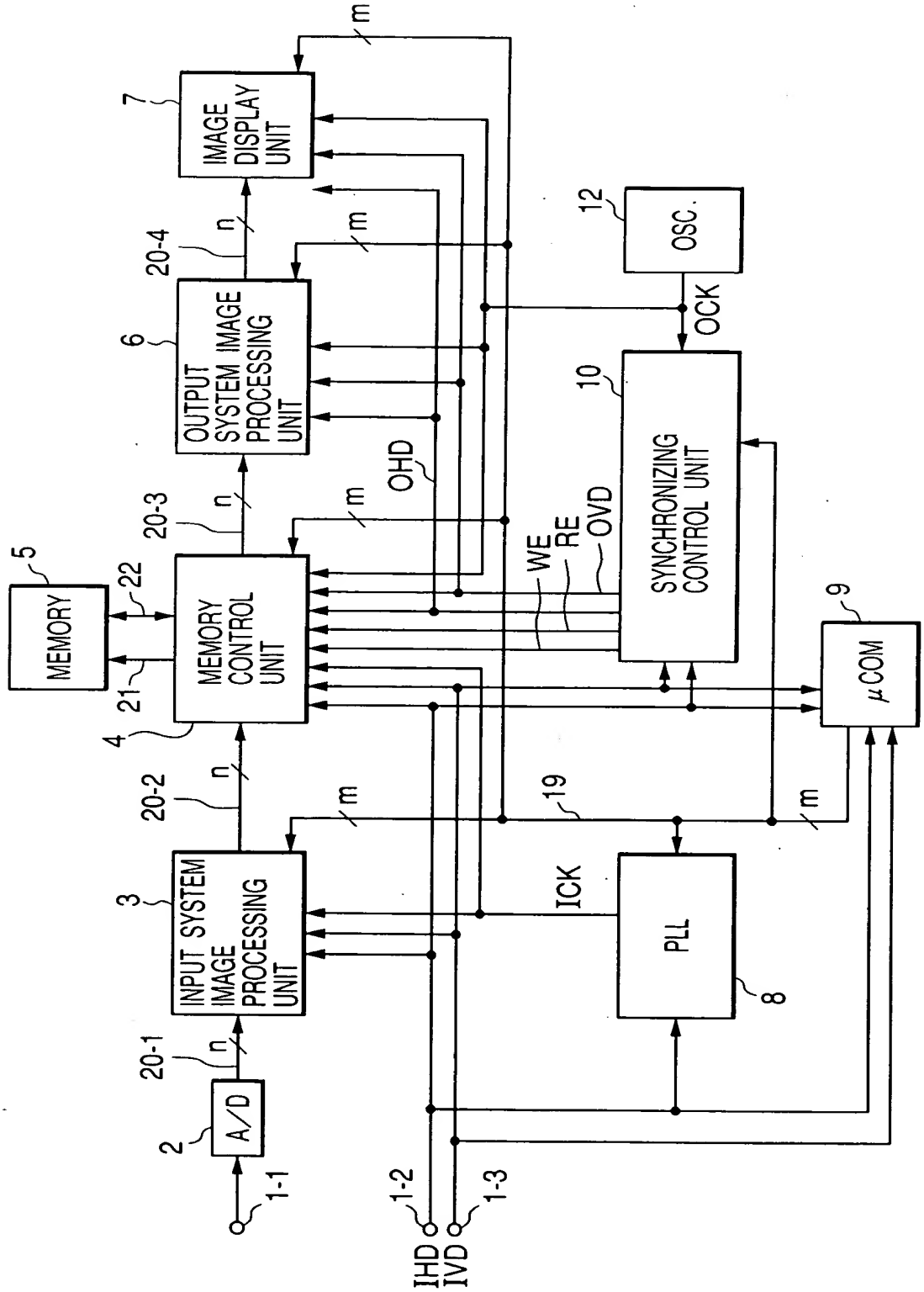
IMAGE DISPLAY UNIT
OUTPUT SYSTEM IMAGE PROCESSING UNIT
MEMORY CONTROL UNIT
MEMORY
INPUT SYSTEM IMAGE PROCESSING UNIT
A/D
SYNCHRONIZING CONTROL UNIT
OSC.
PLL
μCOM
OHD
OVD
WE
RE
OCK
ICK
IHD
IVD
m
n

FIG. 2

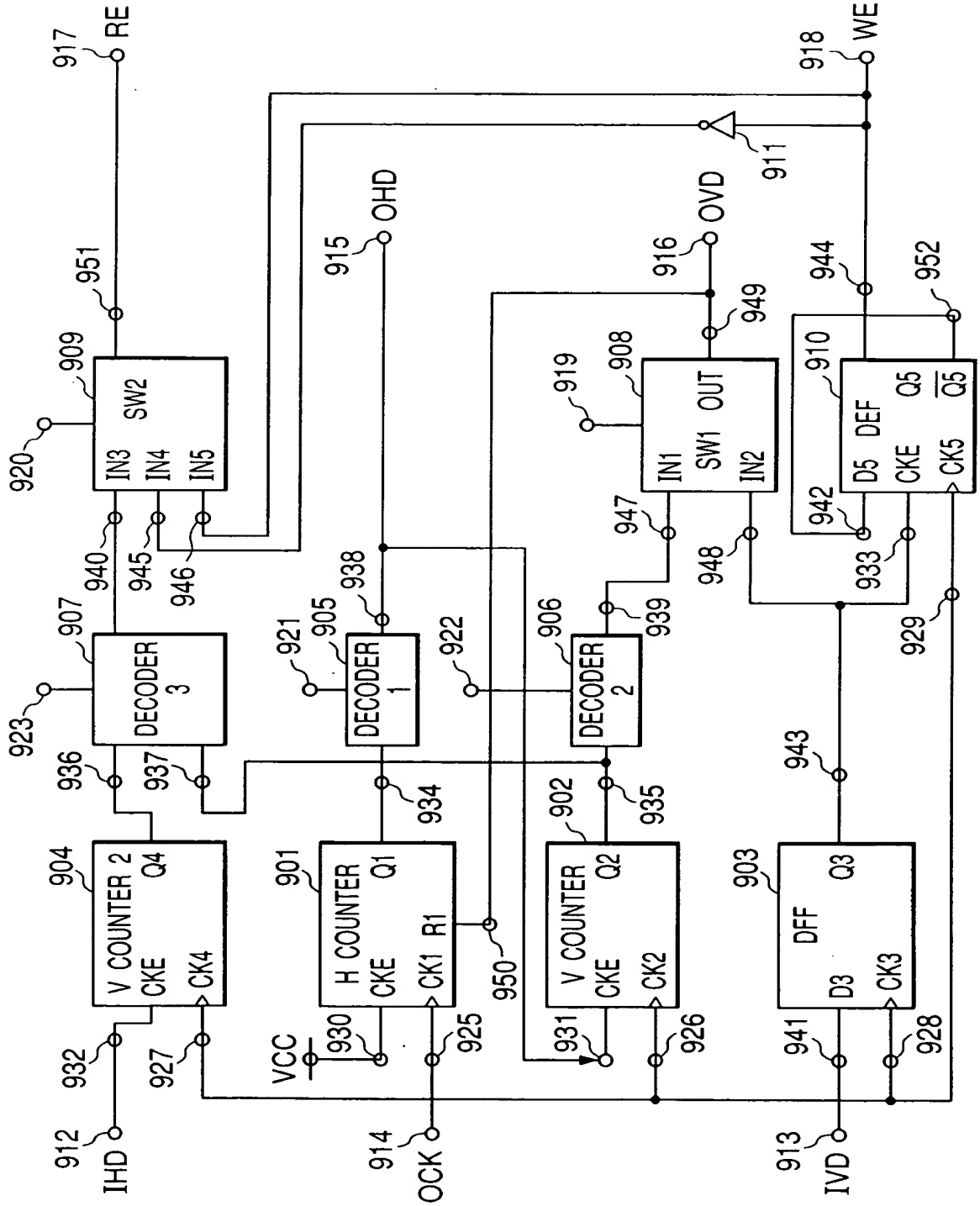
RE
WE
OHD
OVD
IHD
OCK
IVD
VCC
SW2
IN3
IN4
IN5
SW1
OUT
IN1
IN2
DEF
D5
CKE
CK5
Q5
DECODER 3
DECODER 1
DECODER 2
V COUNTER 2
Q4
CK4
H COUNTER
Q1
CK1
R1
V COUNTER
Q2
CK2
DFF
Q3
D3
CK3
917
918
911
915
916
951
944
952
909
908
910
919
920
949
942
947
948
933
940
945
946
938
907
921
905
922
906
939
929
923
936
937
934
902
935
943
904
901
903
932
927
930
925
931
926
941
928
912
914
913
950

FIG. 3

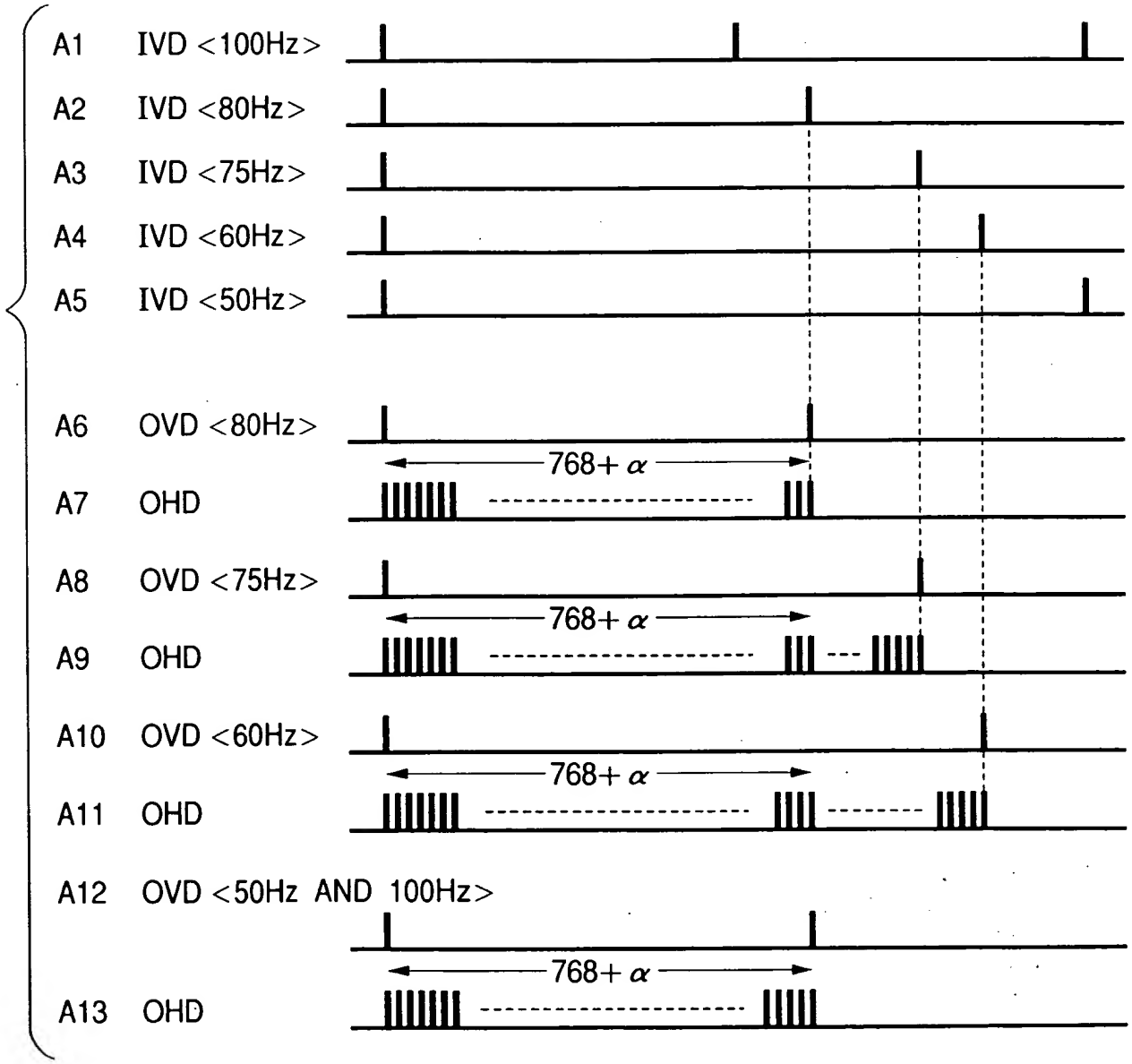
A1 IVD <100Hz>
A2 IVD <80Hz>
A3 IVD <75Hz>
A4 IVD <60Hz>
A5 IVD <50Hz>
A6 OVD <80Hz>
768+ α
A7 OHD
A8 OVD <75Hz>
768+ α
A9 OHD
A10 OVD <60Hz>
768+ α
A11 OHD
A12 OVD <50Hz AND 100Hz>
768+ α
A13 OHD

FIG. 4

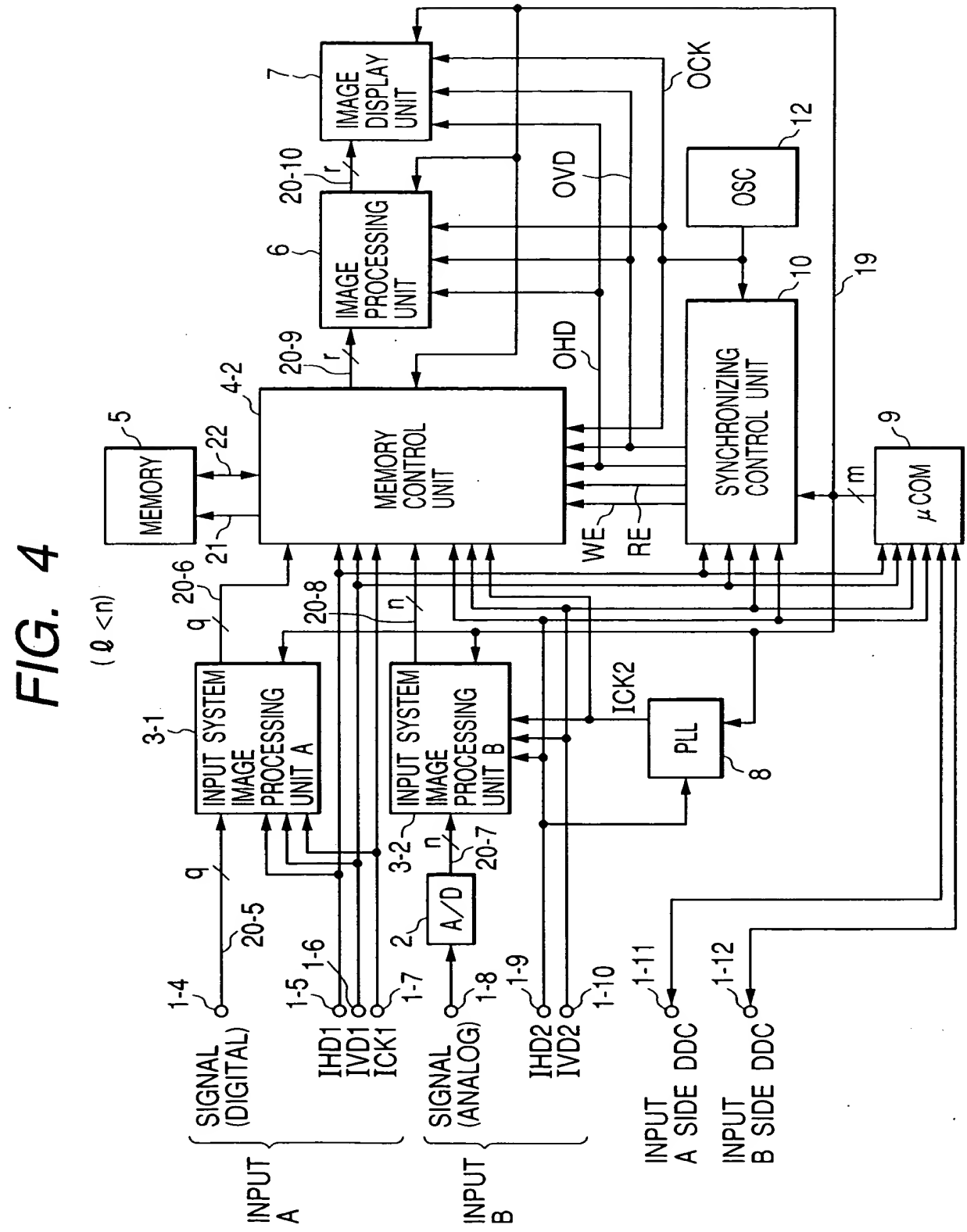
IMAGE DISPLAY UNIT
IMAGE PROCESSING UNIT
MEMORY CONTROL UNIT
MEMORY
SYNCHRONIZING CONTROL UNIT
μCOM
OSC
PLL
A/D
INPUT SYSTEM IMAGE PROCESSING UNIT A
INPUT SYSTEM IMAGE PROCESSING UNIT B
OCK
OVD
OHD
WE
RE
ICK2
SIGNAL (DIGITAL)
IHD1
IVD1
ICK1
SIGNAL (ANALOG)
IHD2
IVD2
INPUT A
INPUT B
INPUT A SIDE DDC
INPUT B SIDE DDC

FIG. 5

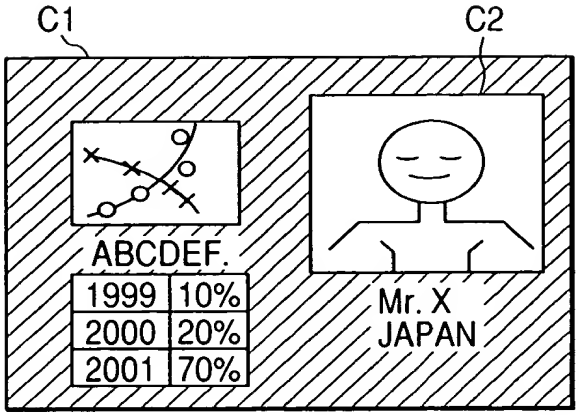
C1
C2
ABCDEF.
1999 10%
2000 20%
2001 70%
Mr. X
JAPAN

FIG. 9

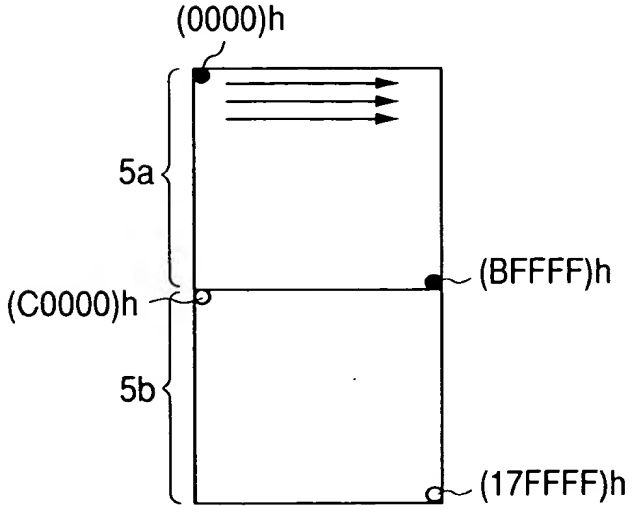
(0000)h
5a
(BFFFF)h
(C0000)h
5b
(17FFFF)h

FIG. 6

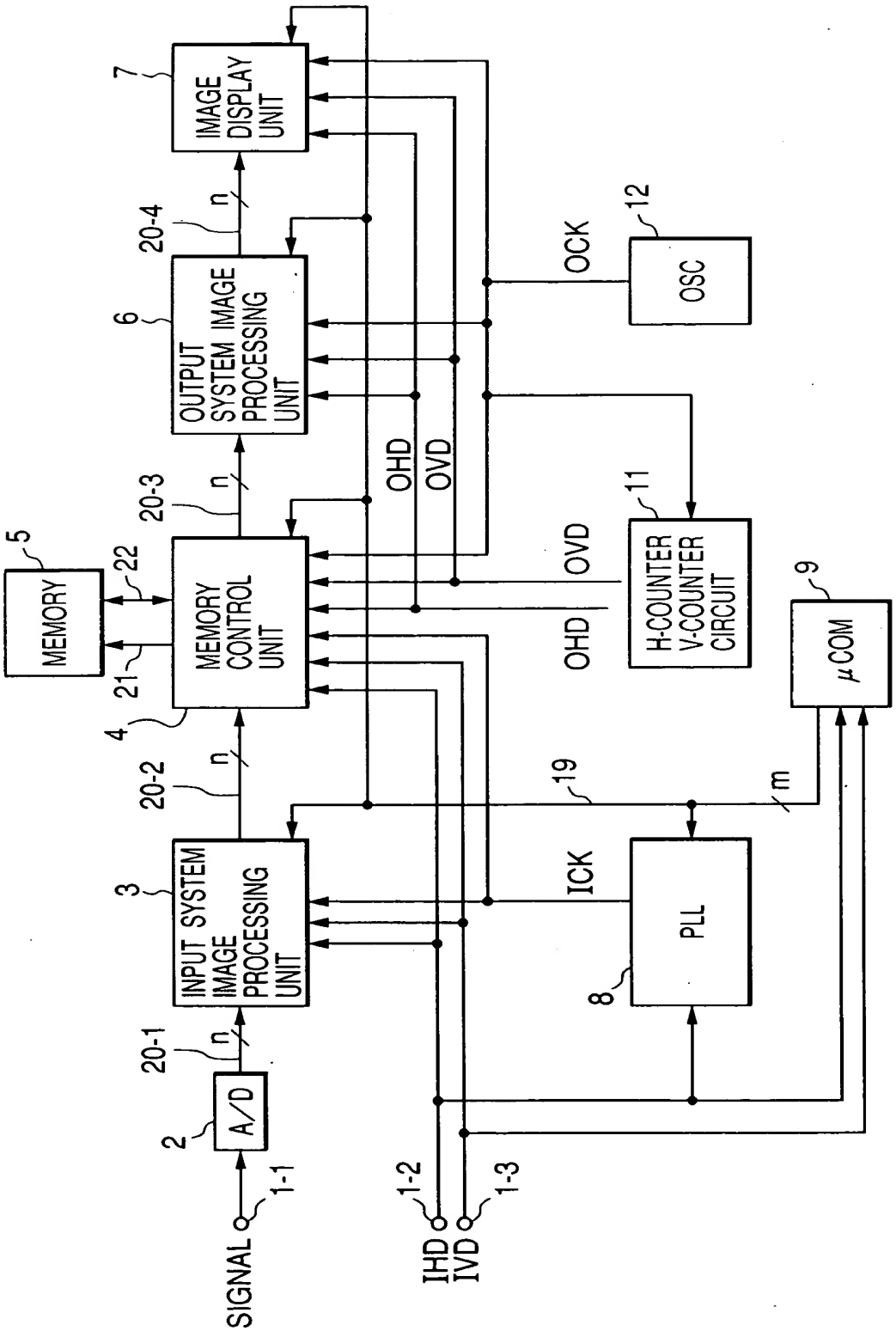
SIGNAL
1-1
A/D
2
20-1
n
INPUT SYSTEM IMAGE PROCESSING UNIT
3
20-2
n
MEMORY CONTROL UNIT
4
21
22
MEMORY
5
20-3
n
OUTPUT SYSTEM IMAGE PROCESSING UNIT
6
20-4
n
IMAGE DISPLAY UNIT
7
PLL
8
ICK
m
19
μCOM
9
H-COUNTER V-COUNTER CIRCUIT
11
OSC
12
OCK
OHD
OVD
IHD
IVD
1-2
1-3

FIG. 7

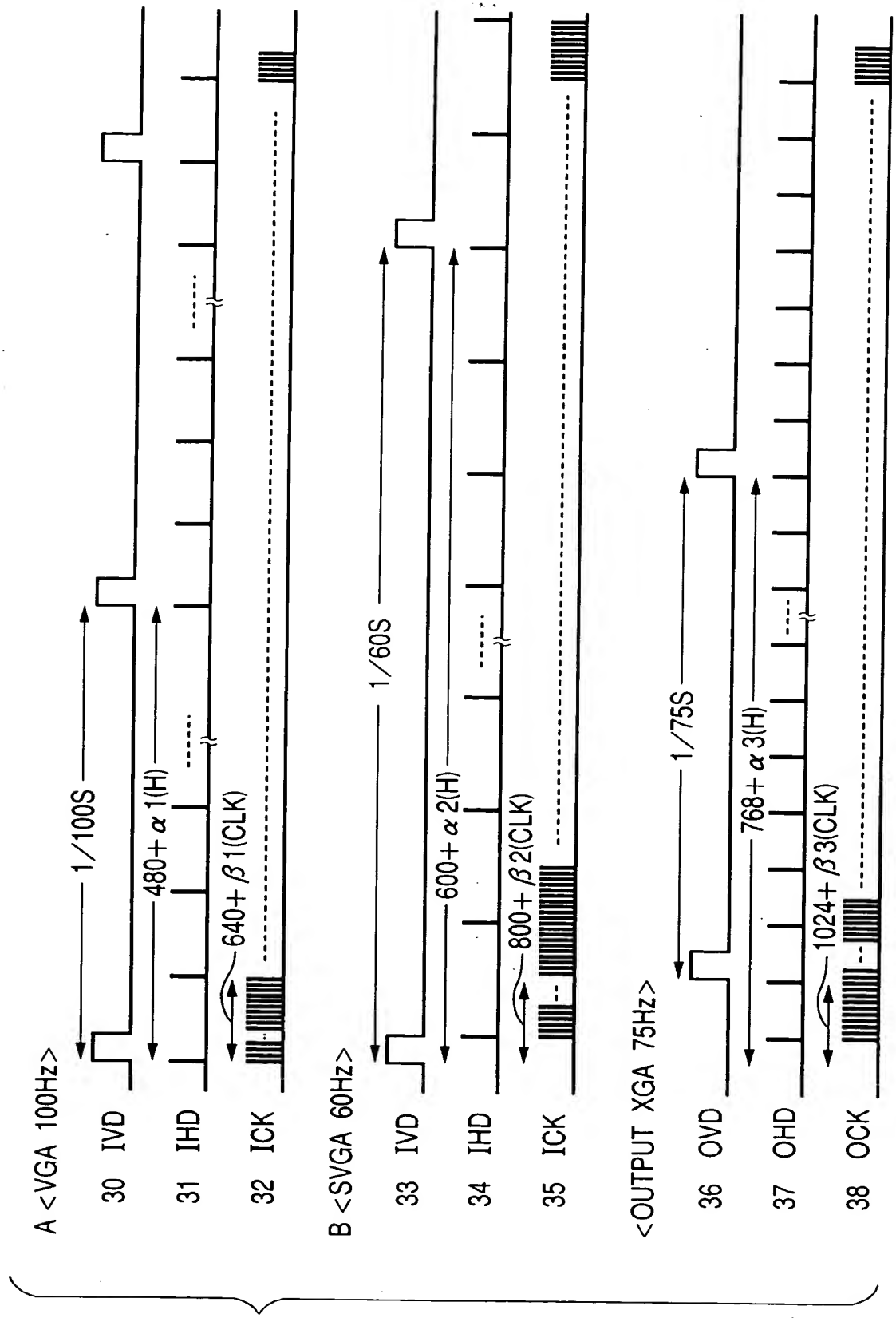
A <VGA 100Hz>
30 IVD
1/100S
480+α1(H)
31 IHD
640+β1(CLK)
32 ICK
B <SVGA 60Hz>
33 IVD
1/60S
600+α2(H)
34 IHD
800+β2(CLK)
35 ICK
<OUTPUT XGA 75Hz>
36 OVD
1/75S
768+α3(H)
37 OHD
1024+β3(CLK)
38 OCK

FIG. 8

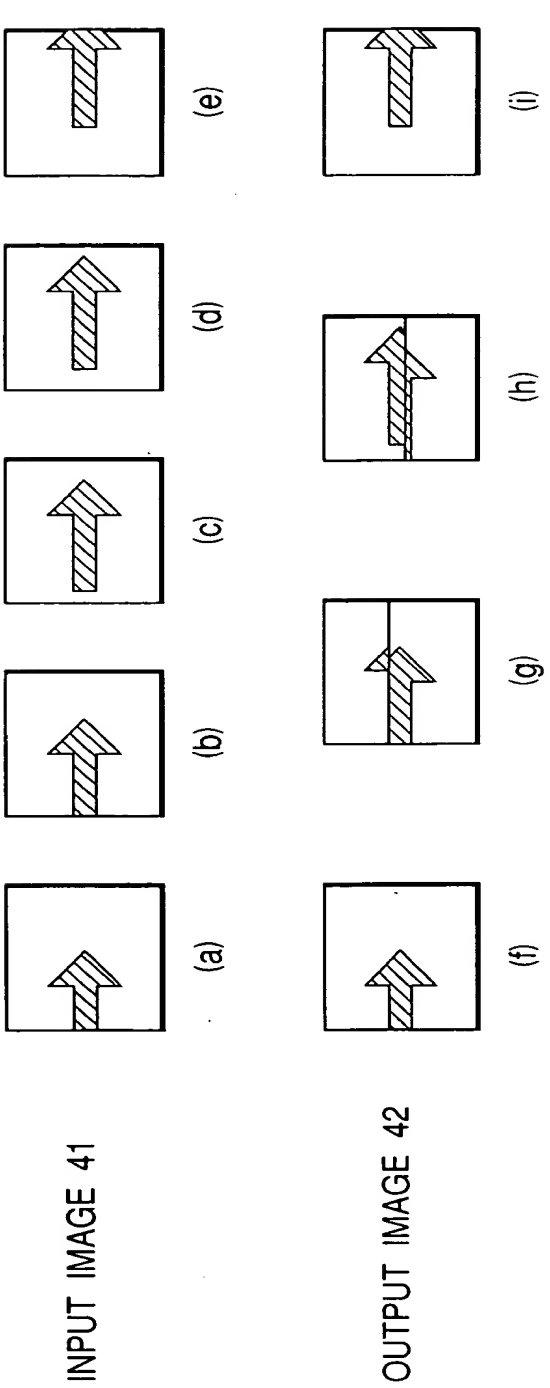

FIG. 10

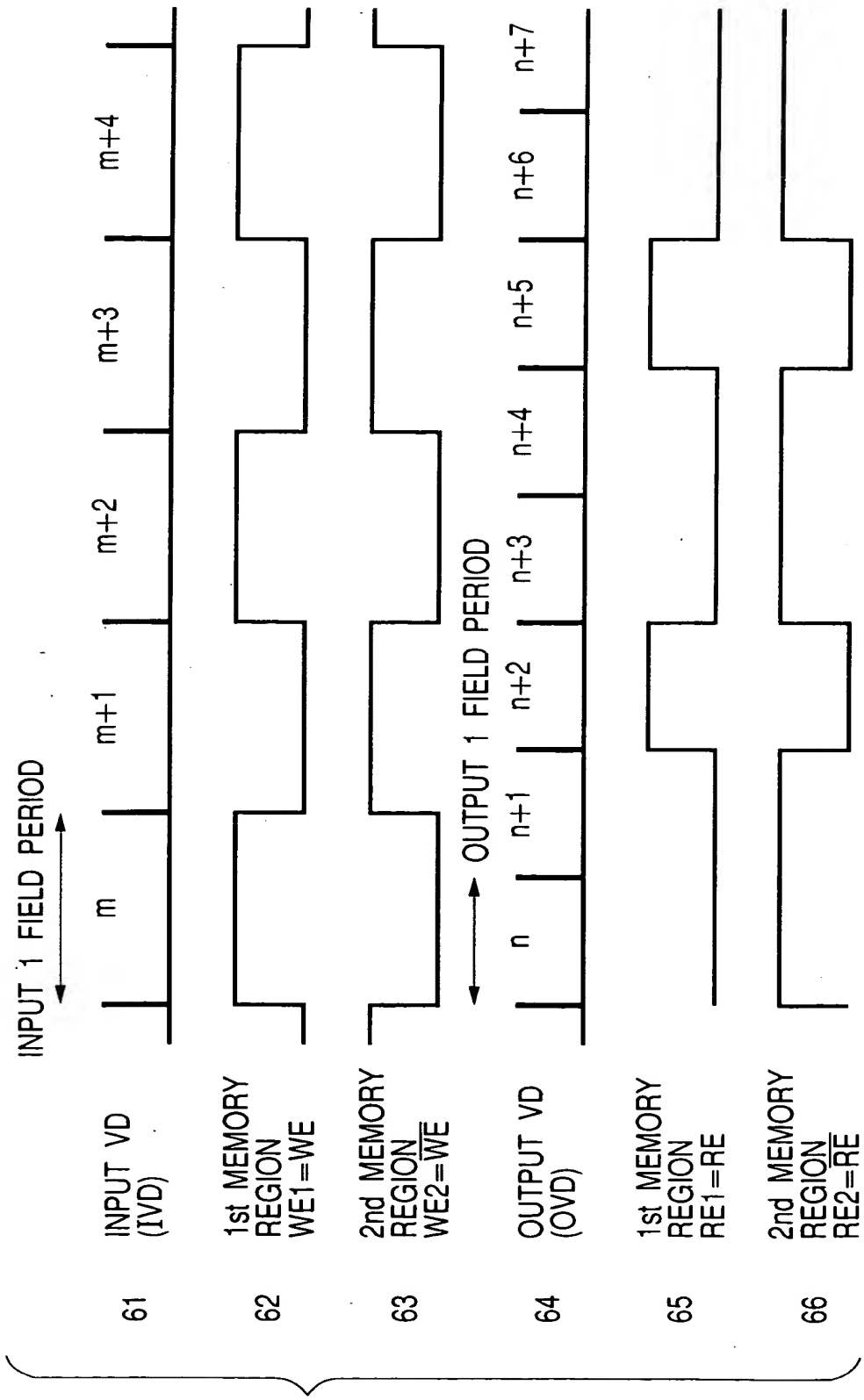
INPUT 1 FIELD PERIOD
m
m+1
m+2
m+3
m+4
61
INPUT VD
(IVD)
62
1st MEMORY
REGION
WE1=WE
63
2nd MEMORY
REGION
WE2=WE
OUTPUT 1 FIELD PERIOD
n
n+1
n+2
n+3
n+4
n+5
n+6
n+7
64
OUTPUT VD
(OVD)
65
1st MEMORY
REGION
RE1=RE
66
2nd MEMORY
REGION
RE2=RE

FIG. 11

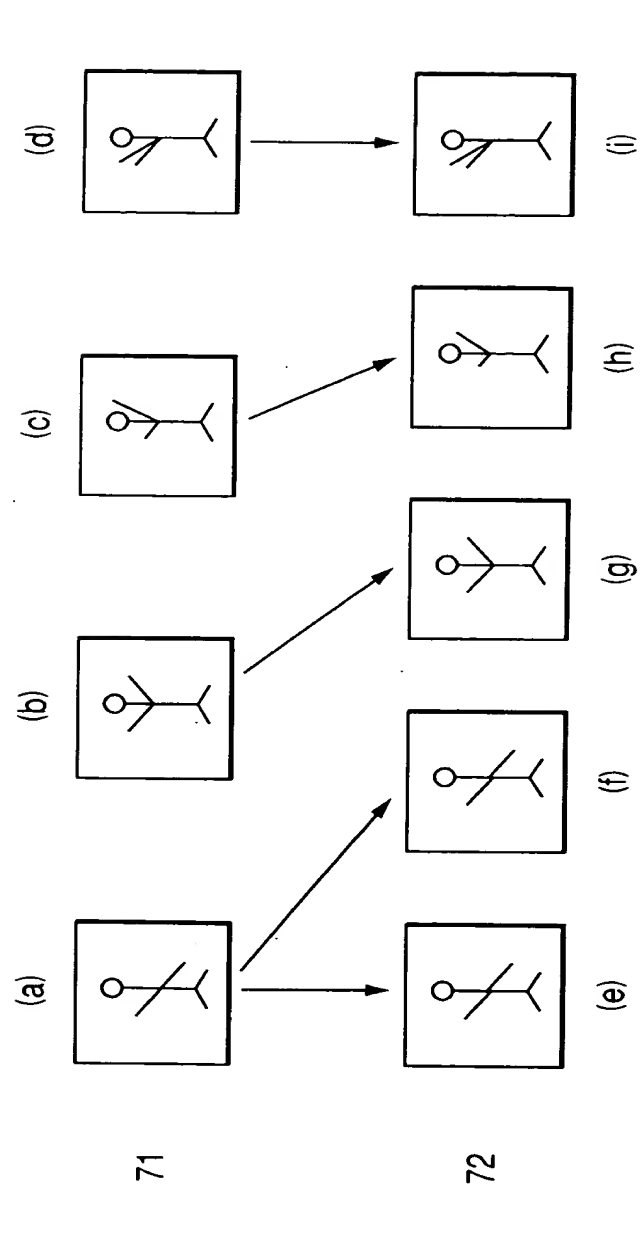

FIG. 12

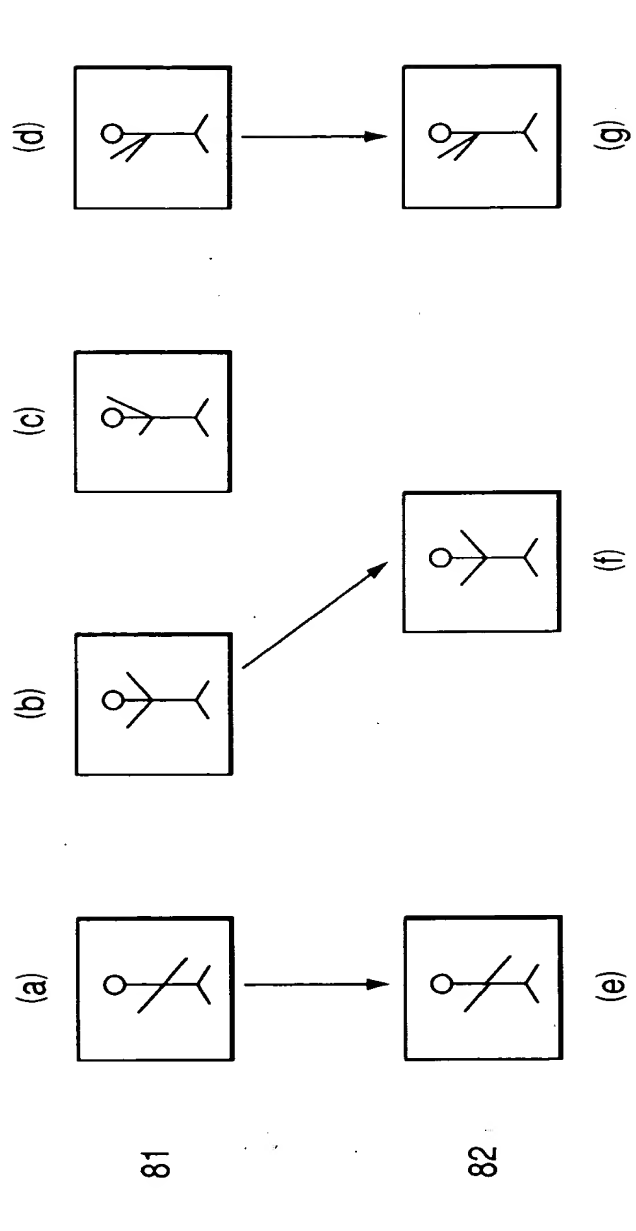

FIG. 13

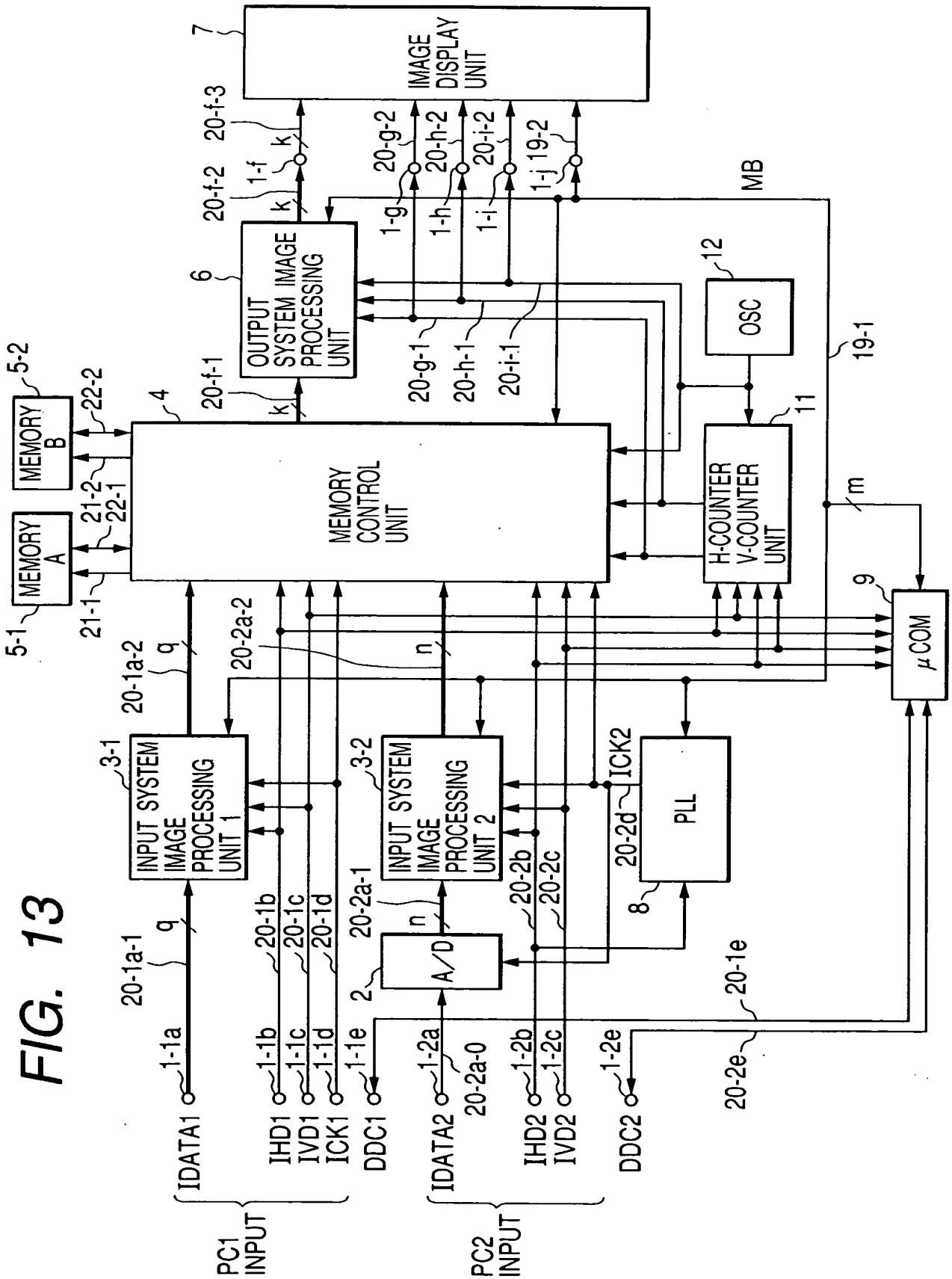
IMAGE DISPLAY UNIT
7
OUTPUT SYSTEM IMAGE PROCESSING UNIT
6
MEMORY CONTROL UNIT
4
MEMORY A
MEMORY B
INPUT SYSTEM IMAGE PROCESSING UNIT 1
INPUT SYSTEM IMAGE PROCESSING UNIT 2
A/D
PLL
OSC
H-COUNTER V-COUNTER UNIT
μCOM
MB
PC1 INPUT
PC2 INPUT
IDATA1
IHD1
IVD1
ICK1
DDC1
IDATA2
IHD2
IVD2
DDC2
ICK2

FIG. 14

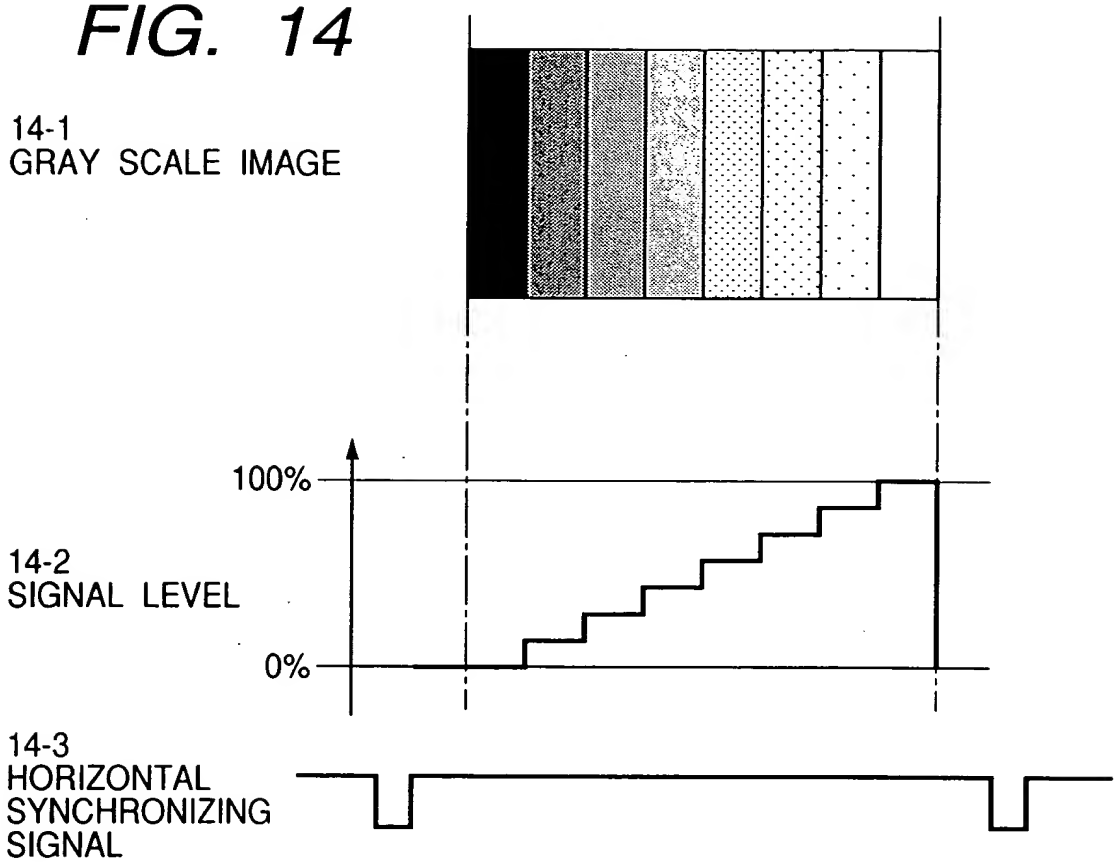
14-1
GRAY SCALE IMAGE
100%
14-2
SIGNAL LEVEL
0%
14-3
HORIZONTAL
SYNCHRONIZING
SIGNAL

FIG. 15

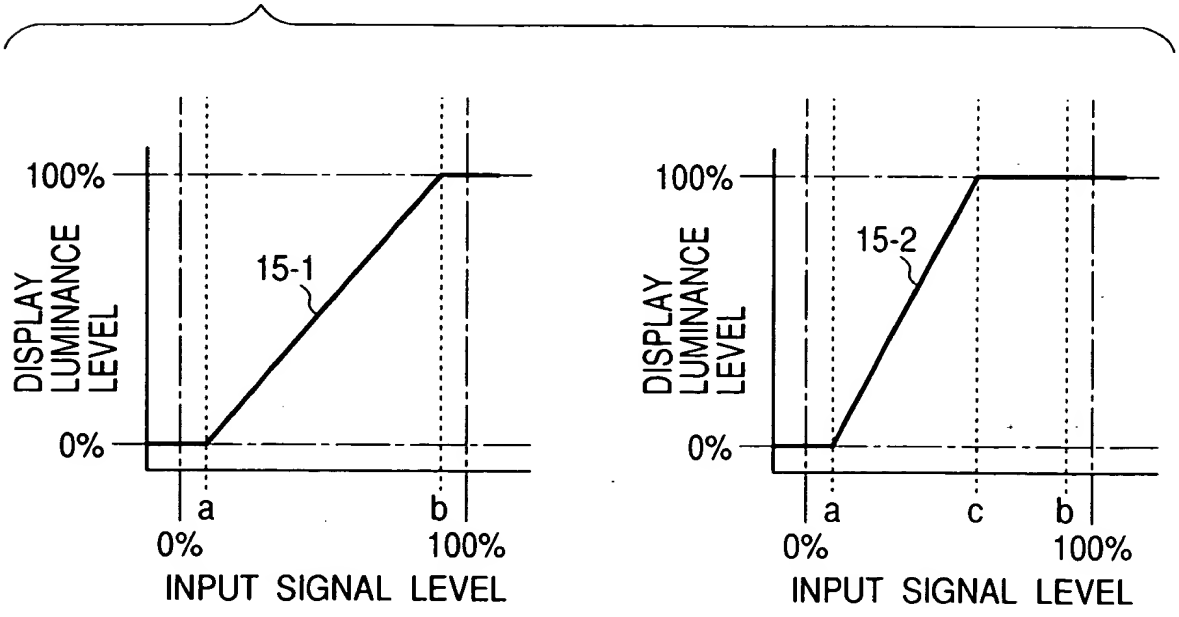
100%
DISPLAY
LUMINANCE
LEVEL
15-1
0%
a
b
0%
100%
INPUT SIGNAL LEVEL
100%
DISPLAY
LUMINANCE
LEVEL
15-2
0%
a
c
b
0%
100%
INPUT SIGNAL LEVEL

FIG. 16

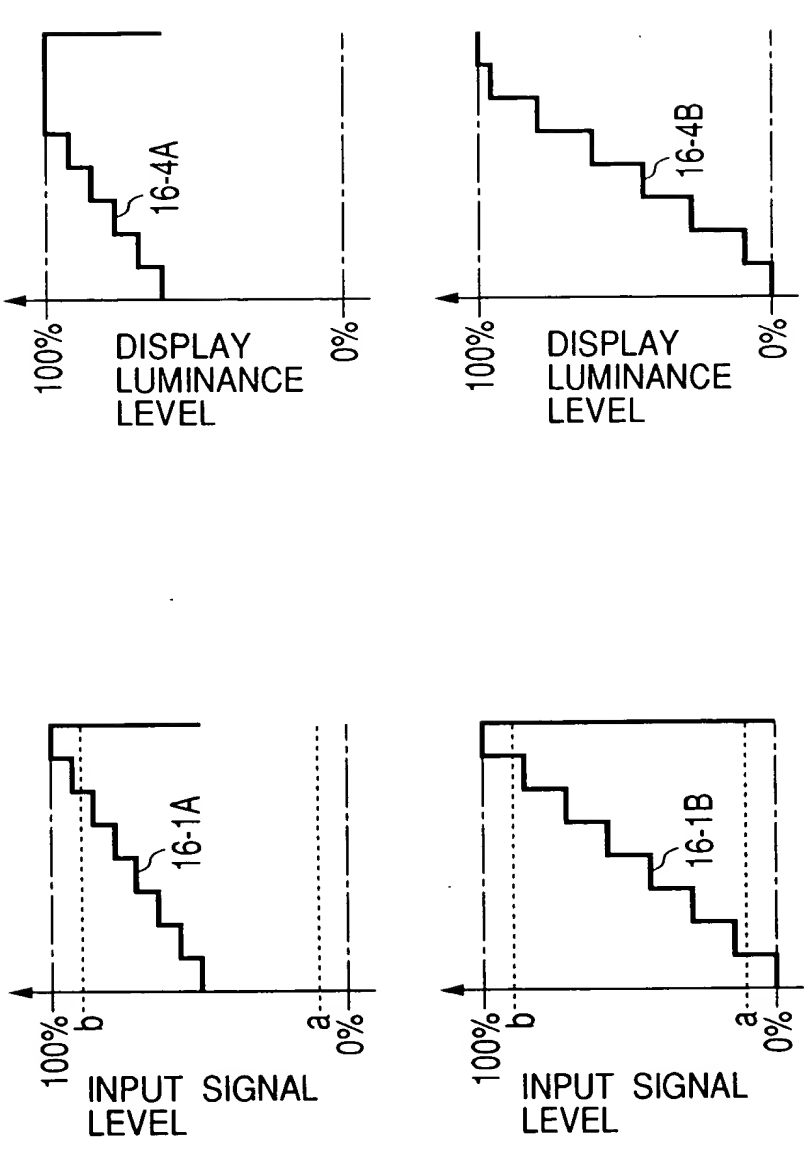
16-4A
100%
DISPLAY
LUMINANCE
LEVEL
0%
16-4B
100%
DISPLAY
LUMINANCE
LEVEL
0%
16-1A
100%
b
a
0%
INPUT SIGNAL
LEVEL
16-1B
100%
b
a
0%
INPUT SIGNAL
LEVEL

FIG. 17

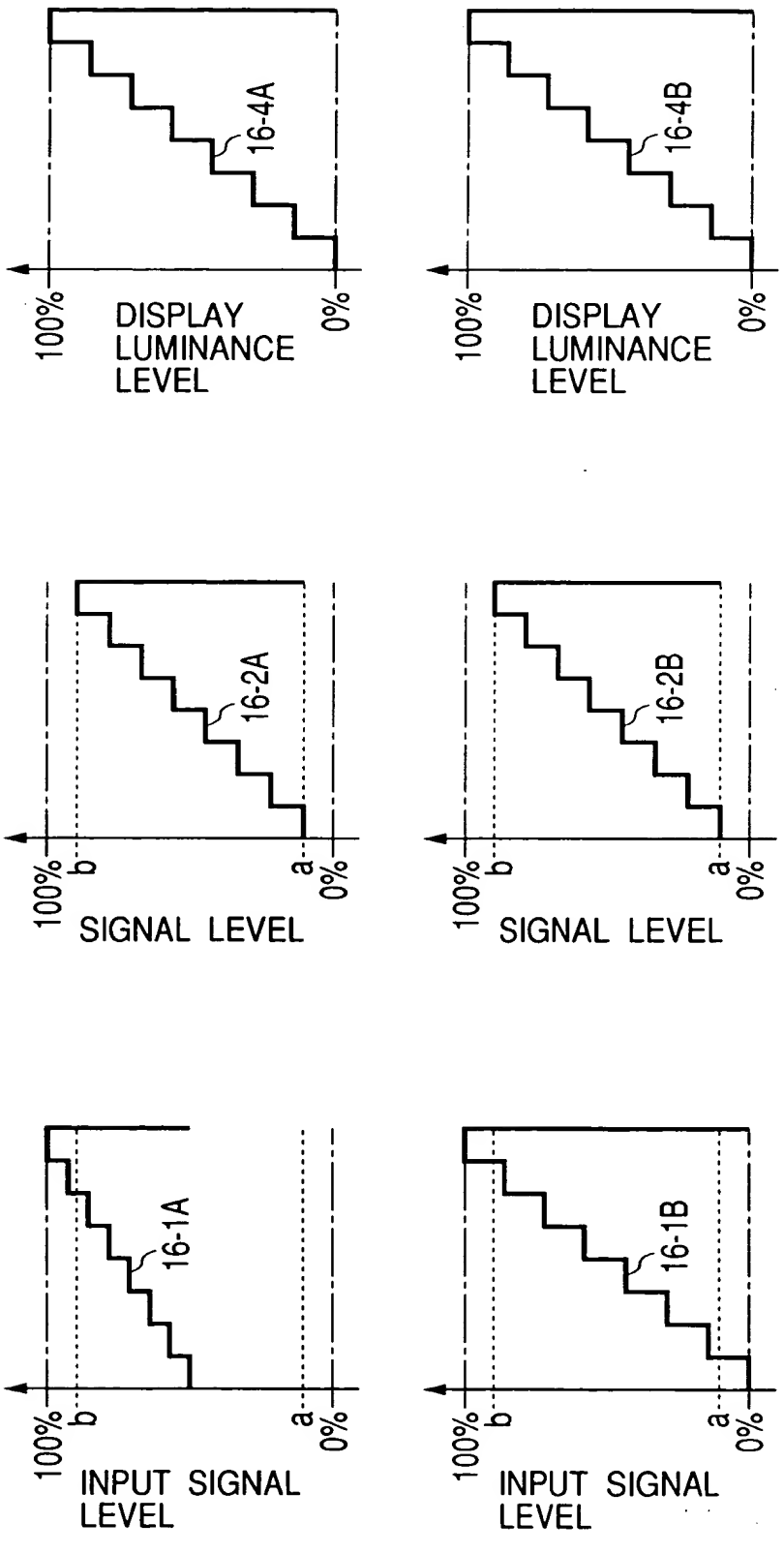
16-4A
100%
DISPLAY LUMINANCE LEVEL
0%
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-2A
100%
b
a
0%
SIGNAL LEVEL
16-2B
100%
b
a
0%
SIGNAL LEVEL
16-1A
100%
b
a
0%
INPUT SIGNAL LEVEL
16-1B
100%
b
a
0%
INPUT SIGNAL LEVEL

FIG. 18

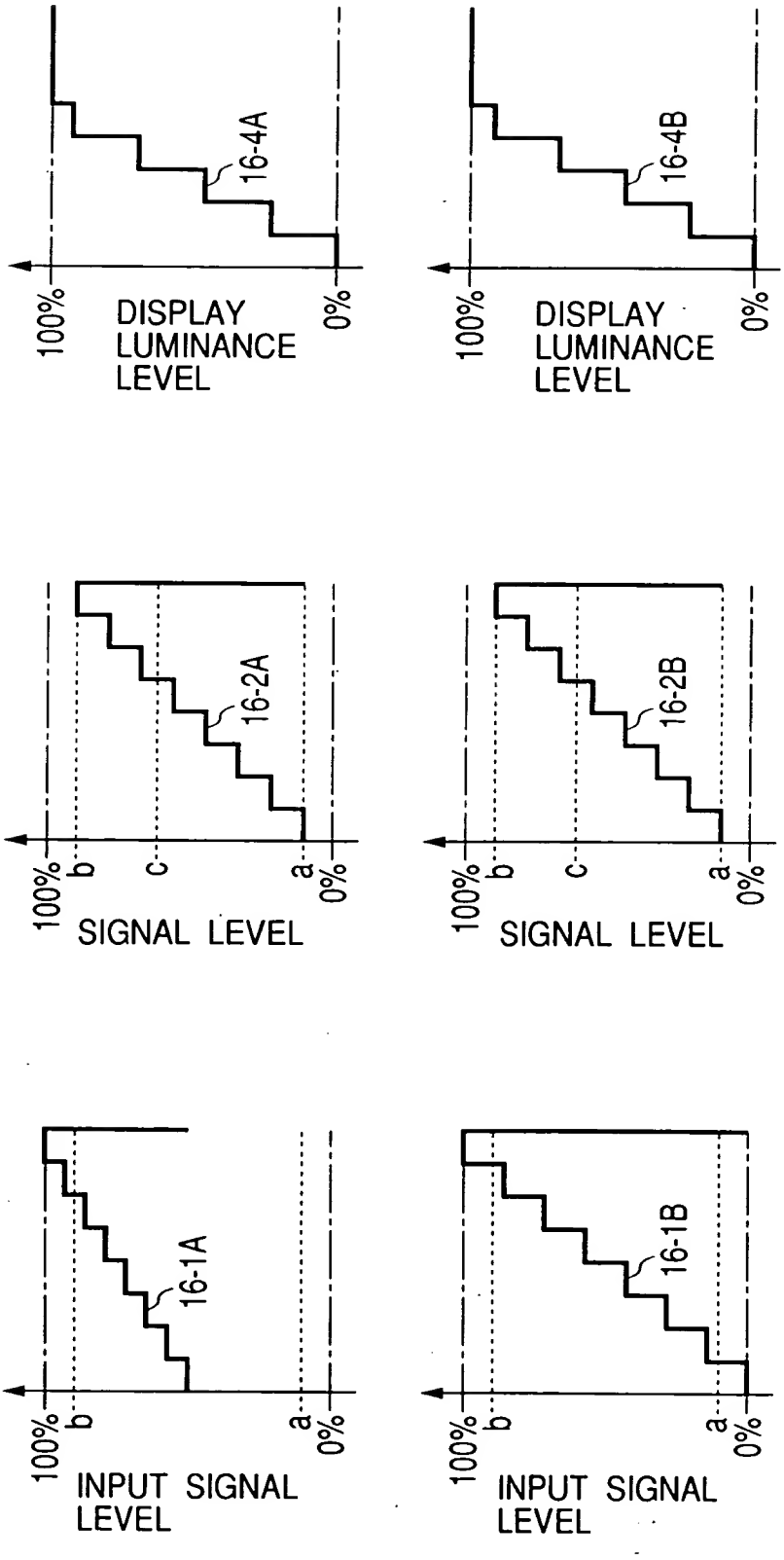
16-4A
100%
DISPLAY LUMINANCE LEVEL
0%
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-2A
100%
b
c
a
0%
SIGNAL LEVEL
16-2B
100%
b
c
a
0%
SIGNAL LEVEL
16-1A
100%
b
a
0%
INPUT SIGNAL LEVEL
16-1B
100%
b
a
0%
INPUT SIGNAL LEVEL

FIG. 19

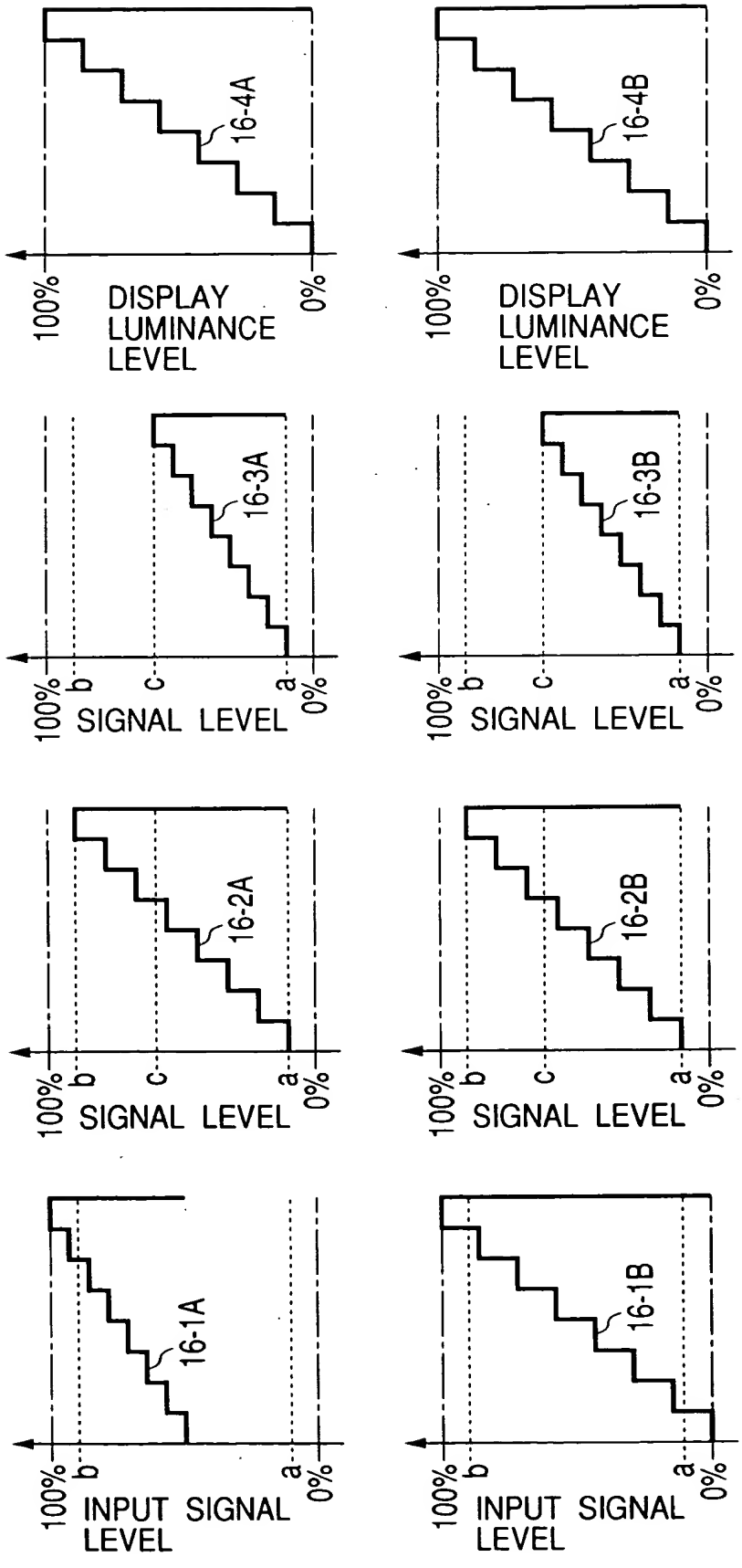
16-4A
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-3A
16-3B
b
c
a
SIGNAL LEVEL
16-2A
16-2B
16-1A
16-1B
INPUT SIGNAL LEVEL

FIG. 20

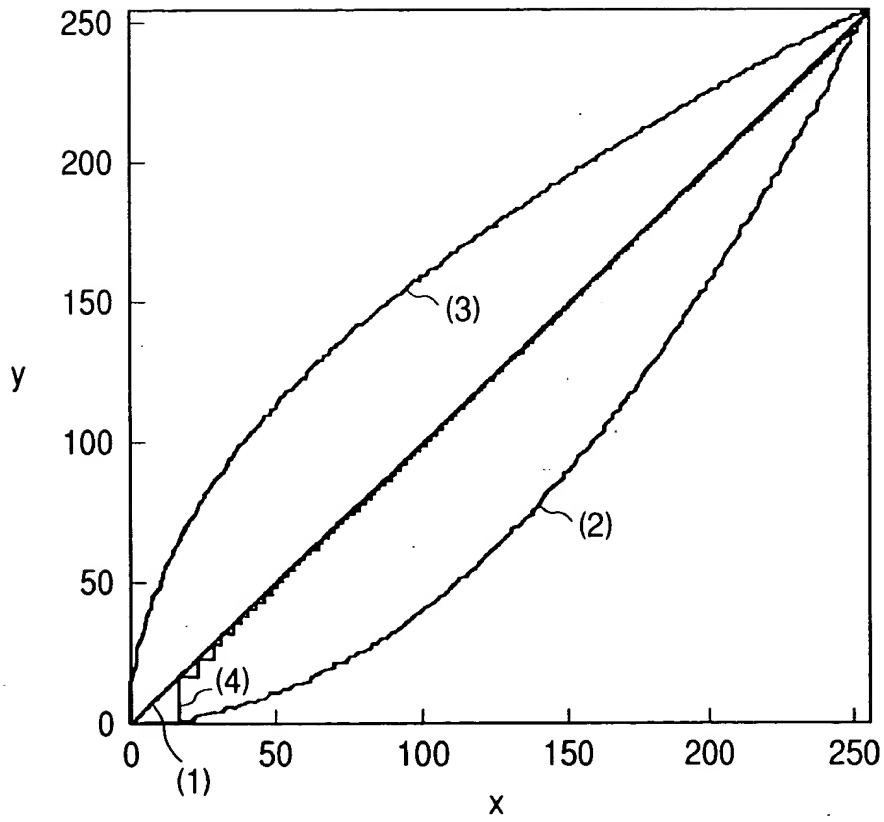

FIG. 21

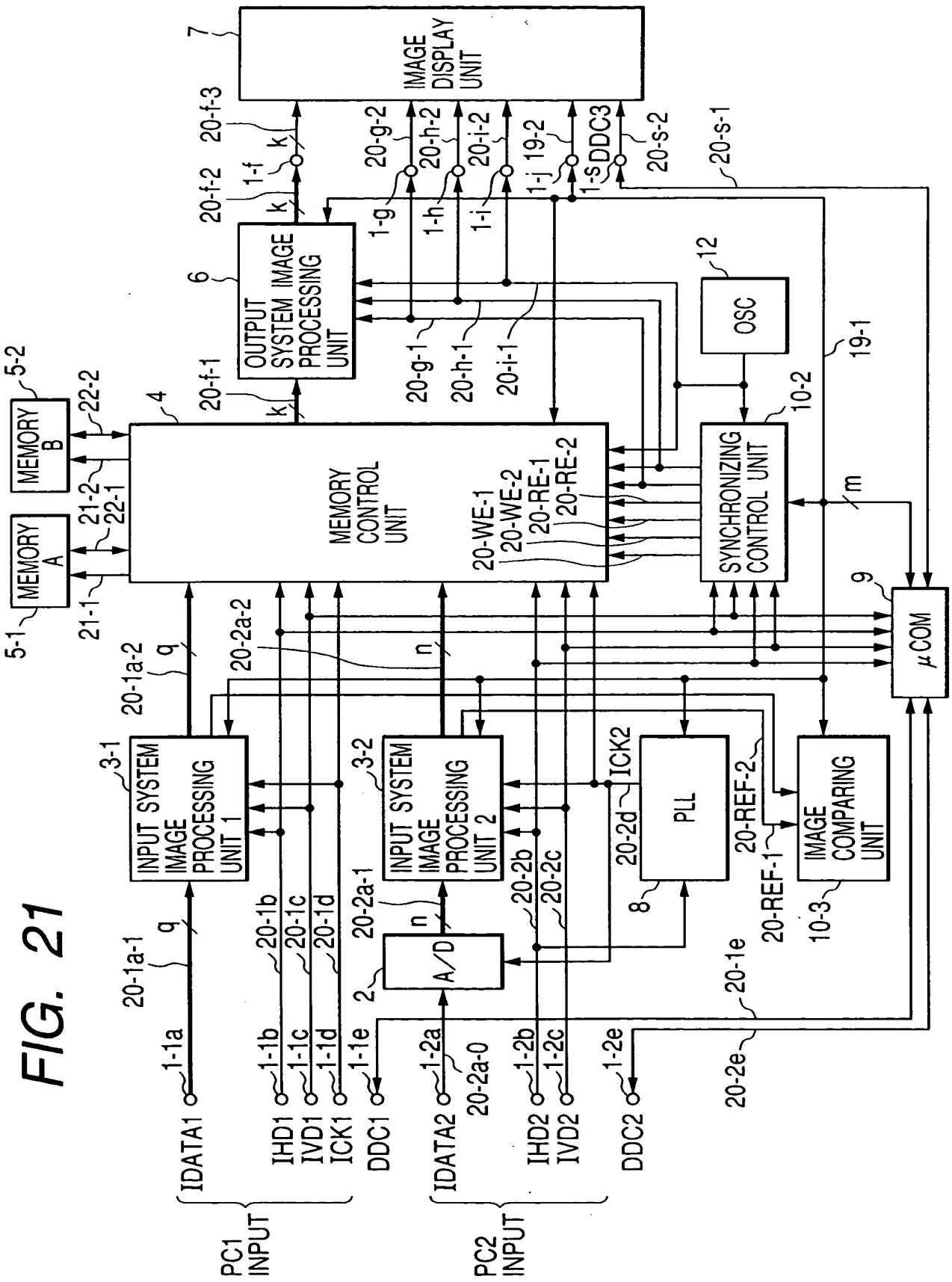
PC1 INPUT
PC2 INPUT
IDATA1
IHD1
IVD1
ICK1
DDC1
IDATA2
IHD2
IVD2
DDC2
INPUT SYSTEM IMAGE PROCESSING UNIT 1
INPUT SYSTEM IMAGE PROCESSING UNIT 2
A/D
MEMORY A
MEMORY B
MEMORY CONTROL UNIT
OUTPUT SYSTEM IMAGE PROCESSING UNIT
IMAGE DISPLAY UNIT
SYNCHRONIZING CONTROL UNIT
OSC
PLL
IMAGE COMPARING UNIT
μCOM
ICK2
20-REF-1
20-REF-2
20-WE-1
20-WE-2
20-RE-1
20-RE-2
20-1a-1
20-1a-2
20-1b
20-1c
20-1d
20-1e
20-2a-0
20-2a-1
20-2a-2
20-2b
20-2c
20-2d
20-2e
20-f-1
20-f-2
20-f-3
20-g-1
20-g-2
20-h-1
20-h-2
20-i-1
20-i-2
20-s-1
20-s-2
19-1
19-2
21-1
21-2
22-1
22-2
1-1a
1-1b
1-1c
1-1d
1-1e
1-2a
1-2b
1-2c
1-2e
1-f
1-g
1-h
1-i
1-j
1-s
2
3-1
3-2
4
5-1
5-2
6
7
8
9
10-2
10-3
12
DDC3
k
m
n
q

FIG. 22

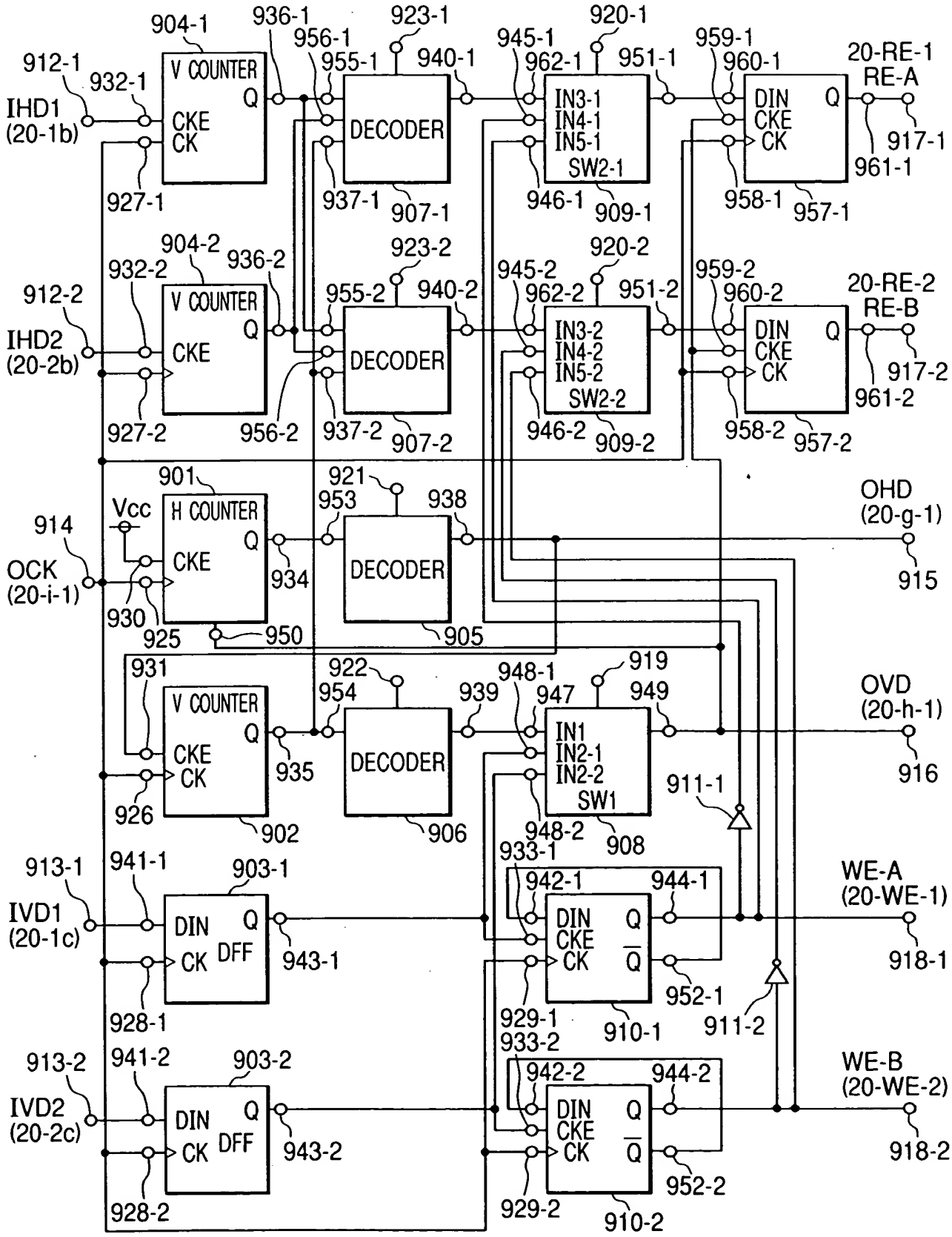
904-1
936-1
923-1
920-1
912-1
932-1
956-1
955-1
940-1
945-1
962-1
951-1
959-1
960-1
20-RE-1
RE-A
IHD1
(20-1b)
V COUNTER
Q
CKE
CK
DECODER
IN3-1
IN4-1
IN5-1
SW2-1
DIN
Q
CKE
CK
917-1
961-1
927-1
937-1
907-1
946-1
909-1
958-1
957-1
904-2
936-2
923-2
920-2
932-2
955-2
940-2
945-2
962-2
951-2
959-2
960-2
20-RE-2
RE-B
912-2
IHD2
(20-2b)
V COUNTER
CKE
DECODER
IN3-2
IN4-2
IN5-2
SW2-2
917-2
961-2
927-2
956-2
937-2
907-2
946-2
909-2
958-2
957-2
901
921
953
938
OHD
(20-g-1)
Vcc
914
H COUNTER
OCK
(20-i-1)
934
915
930
925
950
905
931
922
954
939
948-1
947
919
949
OVD
(20-h-1)
V COUNTER
CKE
CK
935
DECODER
IN1
IN2-1
IN2-2
SW1
916
926
902
906
911-1
948-2
908
933-1
913-1
941-1
903-1
942-1
944-1
WE-A
(20-WE-1)
IVD1
(20-1c)
DIN
Q
CK
DFF
943-1
928-1
929-1
952-1
911-2
910-1
918-1
933-2
913-2
941-2
903-2
942-2
944-2
WE-B
(20-WE-2)
IVD2
(20-2c)
943-2
928-2
929-2
952-2
910-2
918-2

FIG. 23

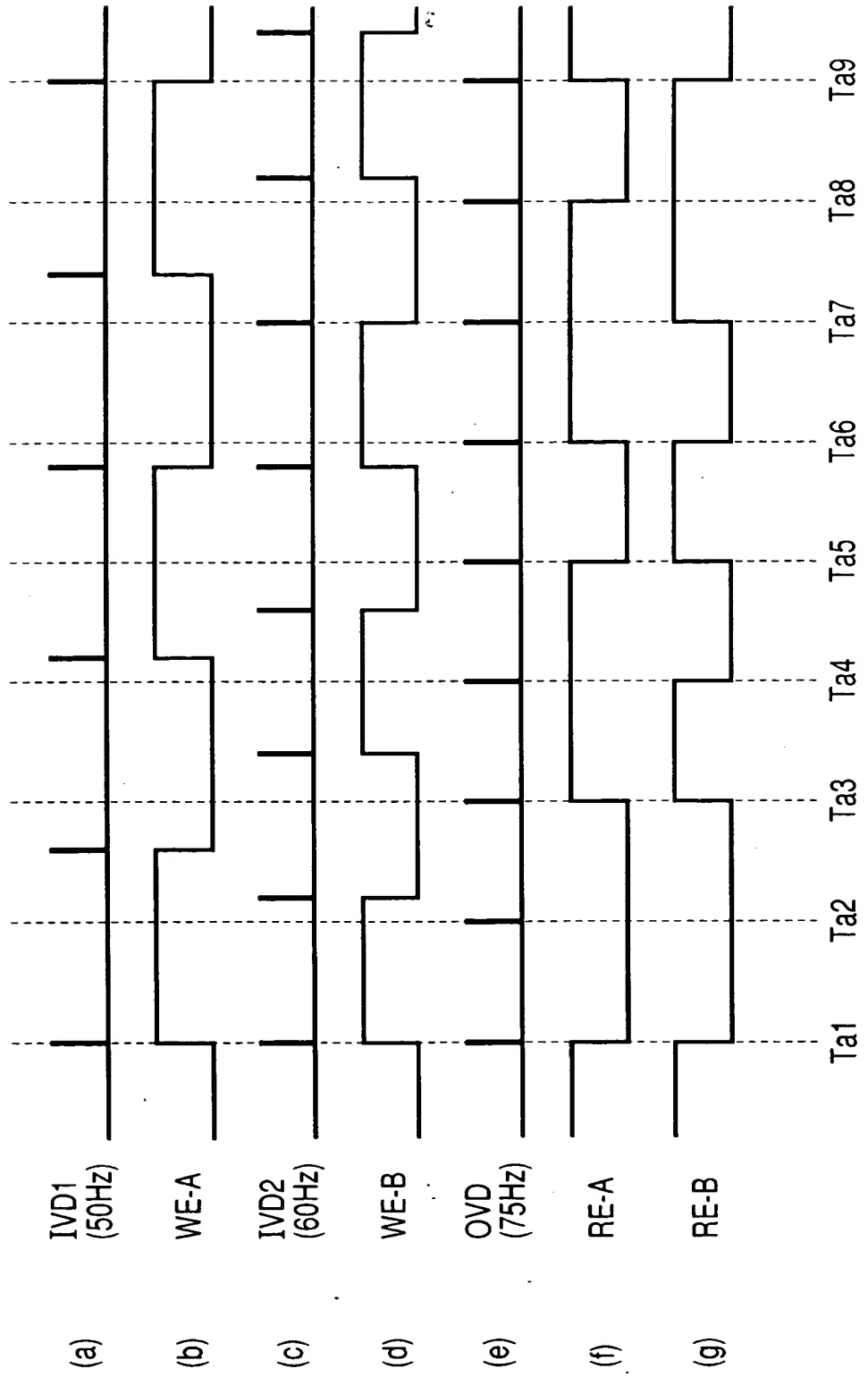
(a)
IVD1 (50Hz)
(b)
WE-A
(c)
IVD2 (60Hz)
(d)
WE-B
(e)
OVD (75Hz)
(f)
RE-A
(g)
RE-B
Ta1
Ta2
Ta3
Ta4
Ta5
Ta6
Ta7
Ta8
Ta9

FIG. 24

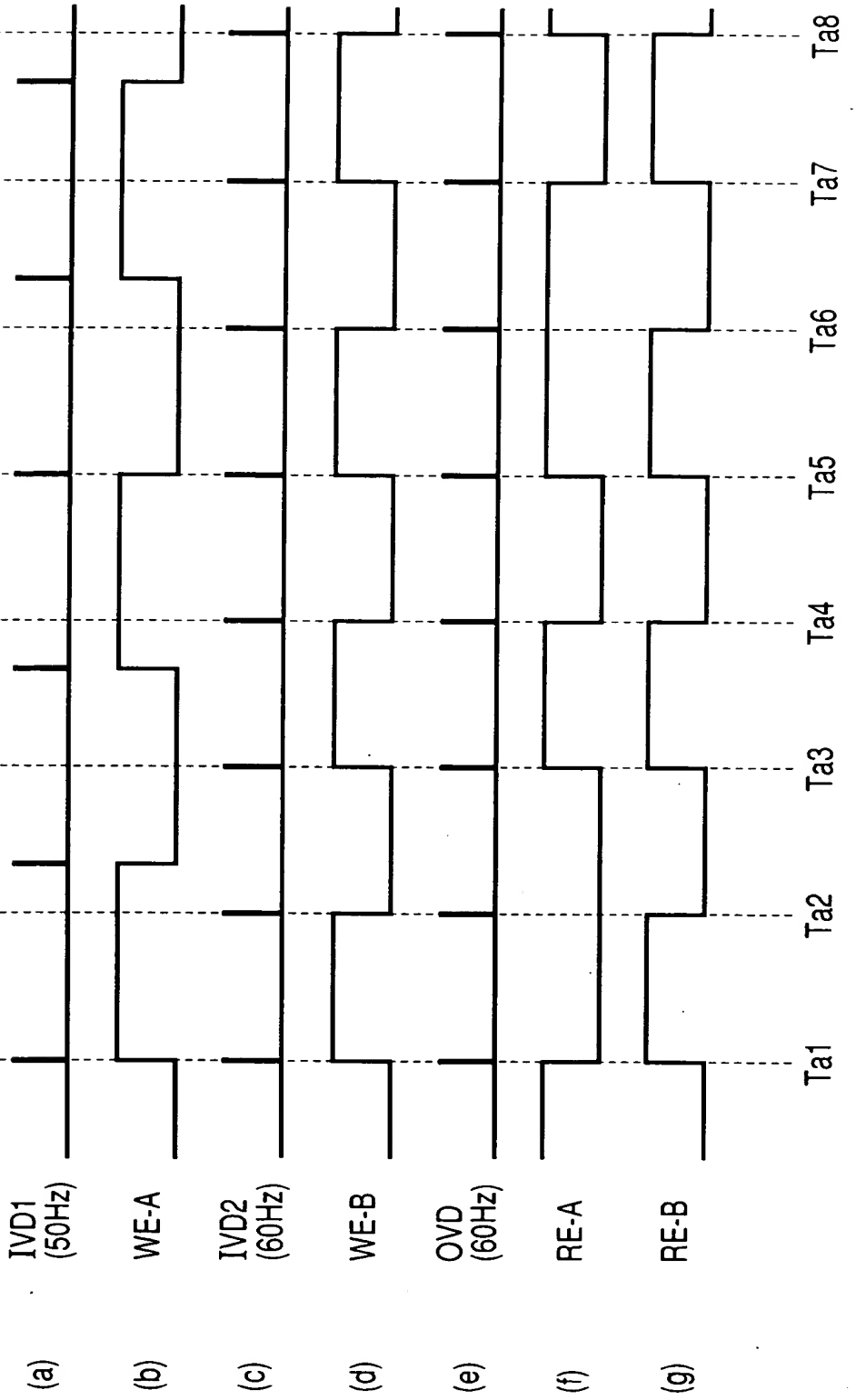
(a)
IVD1 (50Hz)
(b)
WE-A
(c)
IVD2 (60Hz)
(d)
WE-B
(e)
OVD (60Hz)
(f)
RE-A
(g)
RE-B
Ta1
Ta2
Ta3
Ta4
Ta5
Ta6
Ta7
Ta8

FIG. 25

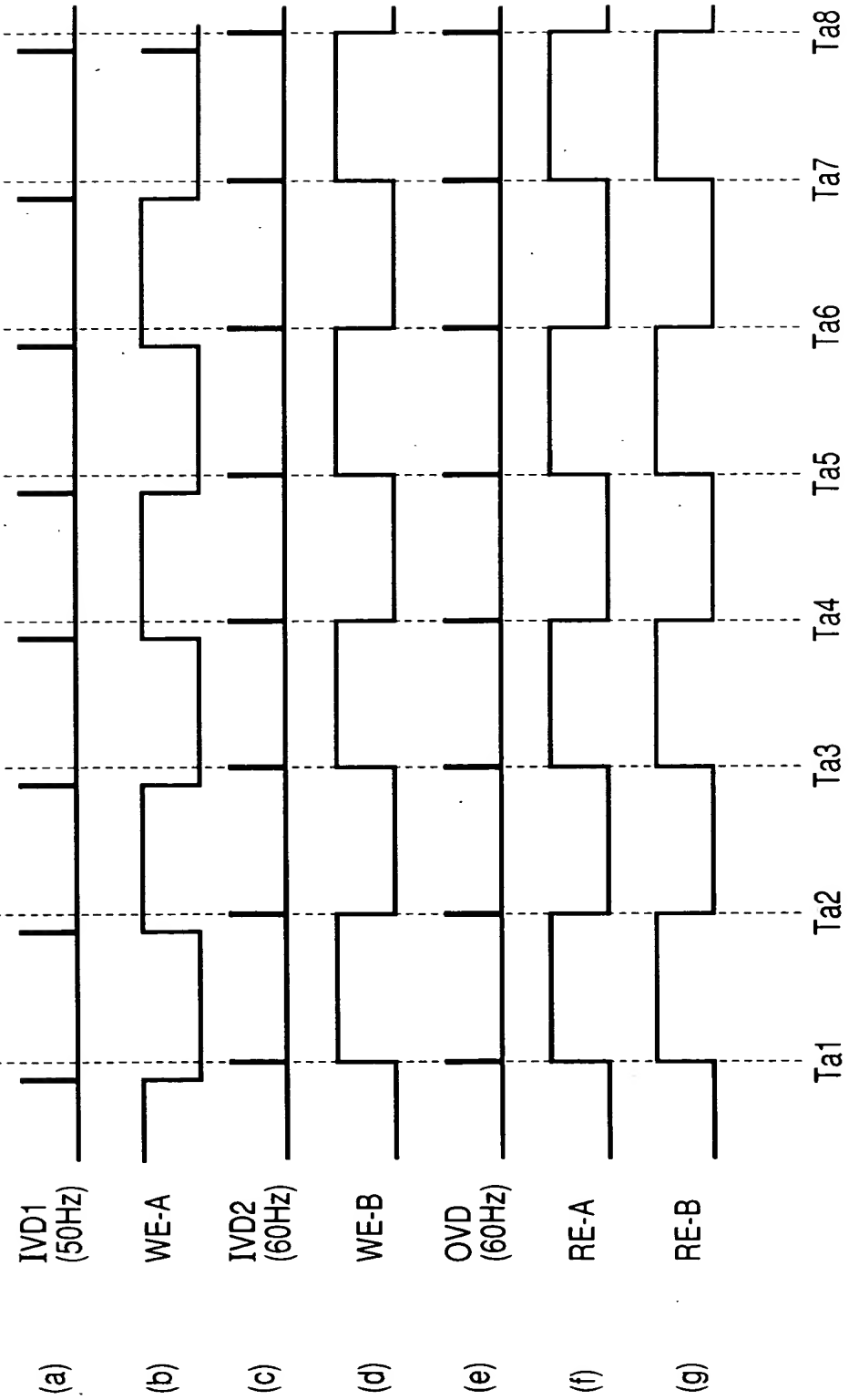
(a)
IVD1 (50Hz)
(b)
WE-A
(c)
IVD2 (60Hz)
(d)
WE-B
(e)
OVD (60Hz)
(f)
RE-A
(g)
RE-B
Ta1
Ta2
Ta3
Ta4
Ta5
Ta6
Ta7
Ta8

FIG. 26

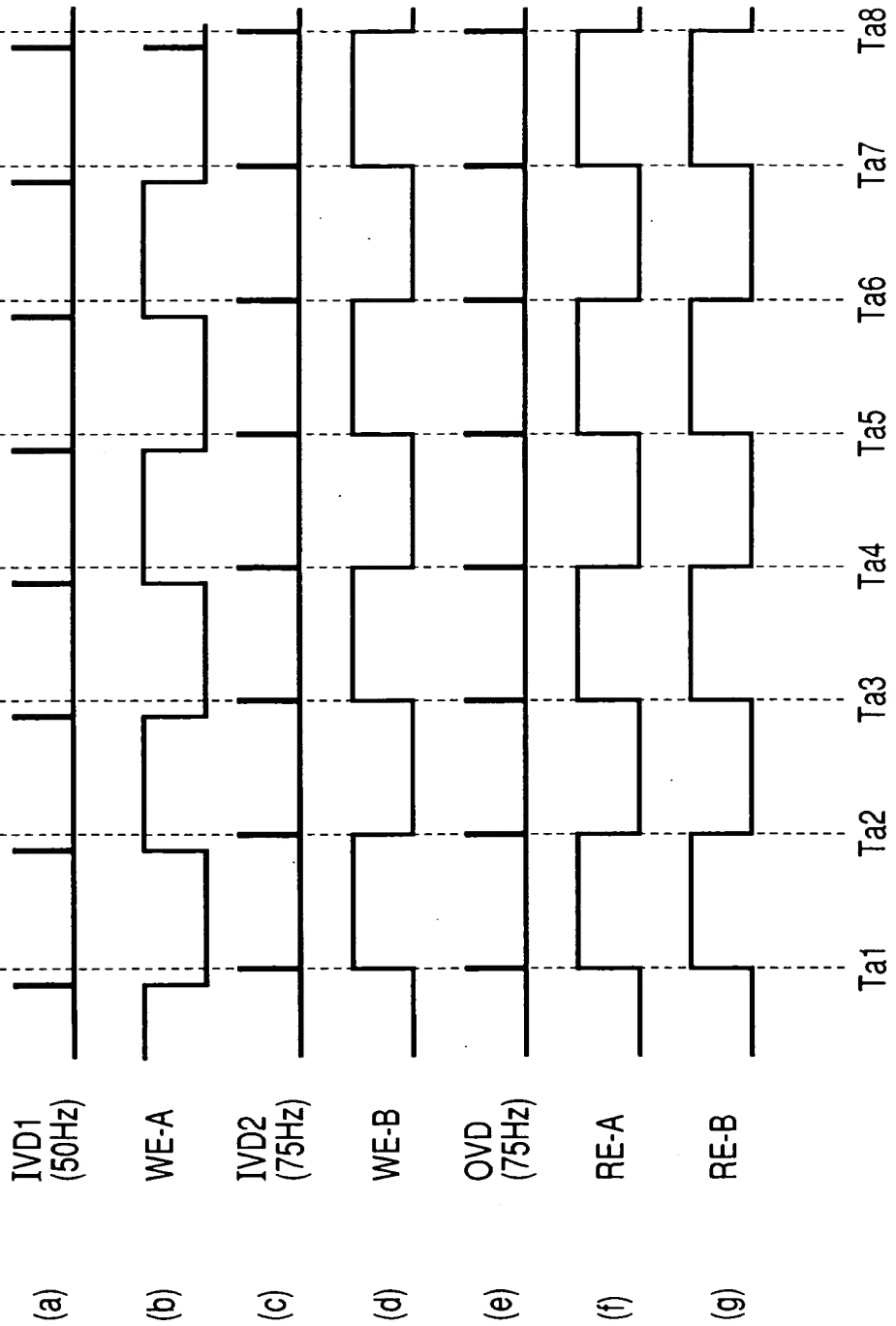
Ta1
Ta2
Ta3
Ta4
Ta5
Ta6
Ta7
Ta8
(a) IVD1 (50Hz)
(b) WE-A
(c) IVD2 (75Hz)
(d) WE-B
(e) OVD (75Hz)
(f) RE-A
(g) RE-B

FIG. 27

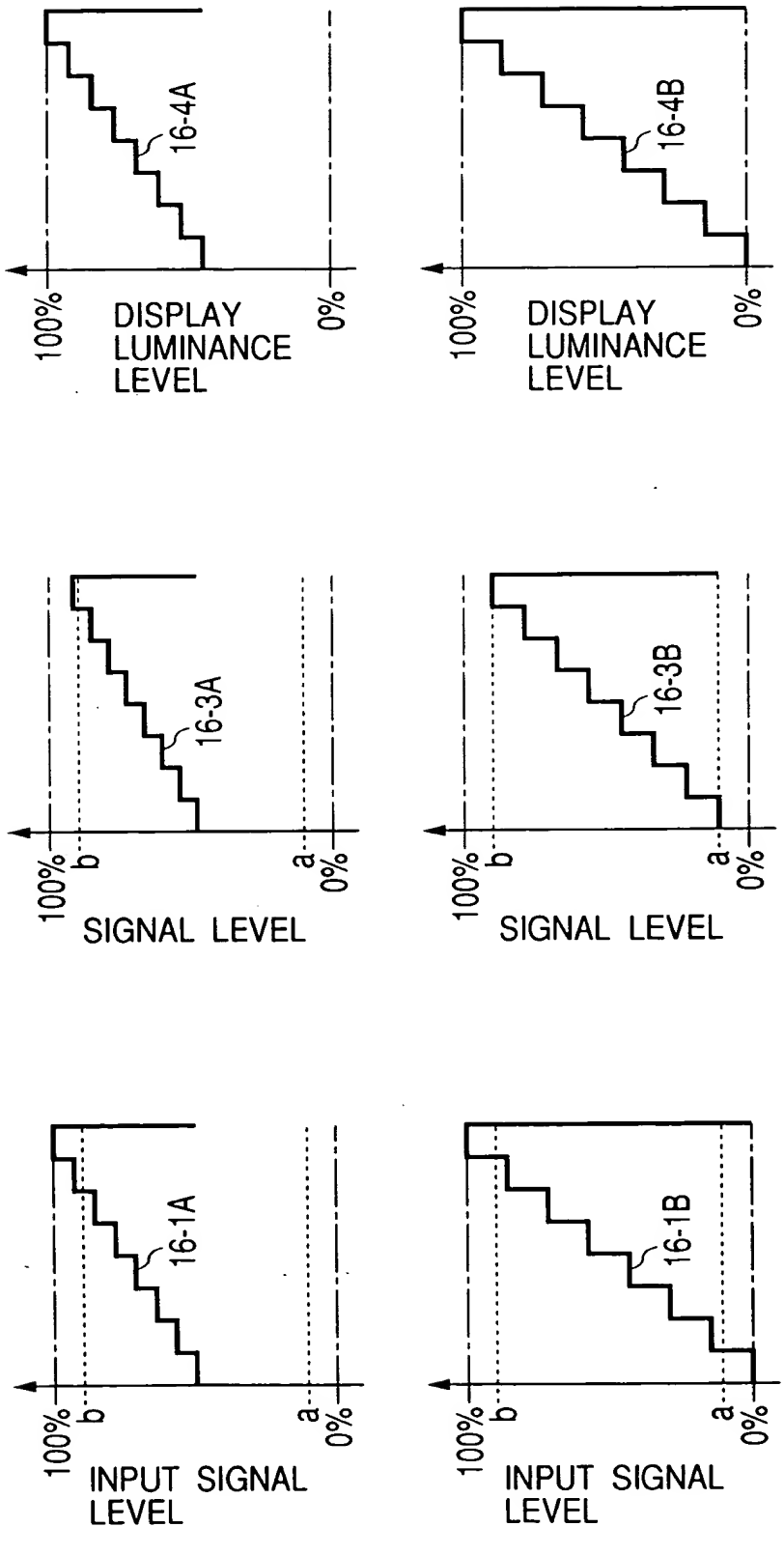
16-4A
100%
DISPLAY LUMINANCE LEVEL
0%
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-3A
100%
b
a
0%
SIGNAL LEVEL
16-3B
100%
b
a
0%
SIGNAL LEVEL
16-1A
100%
b
a
0%
INPUT SIGNAL LEVEL
16-1B
100%
b
a
0%
INPUT SIGNAL LEVEL

FIG. 28

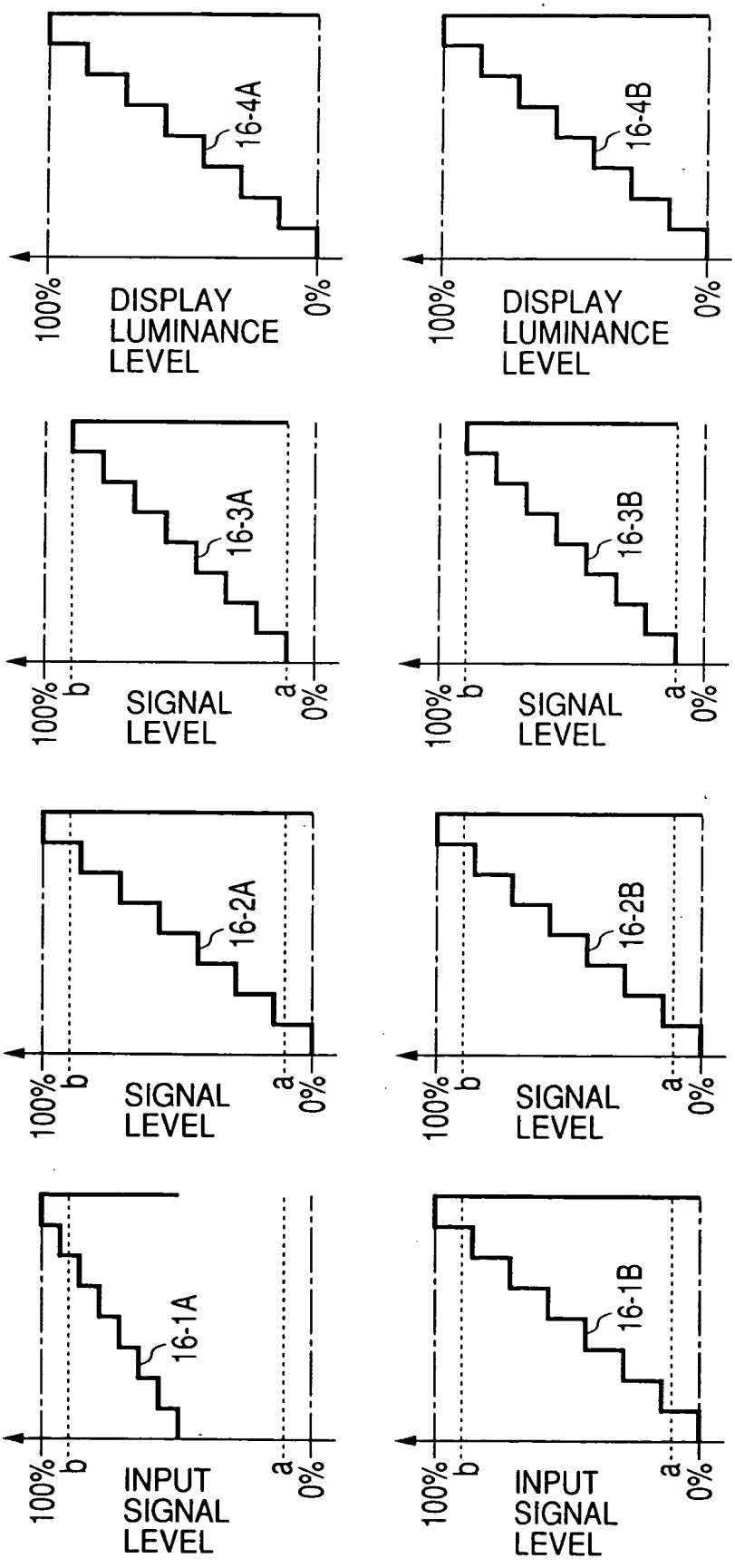
16-4A
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-3A
16-3B
b
SIGNAL LEVEL
a
16-2A
16-2B
16-1A
16-1B
INPUT SIGNAL LEVEL

FIG. 29

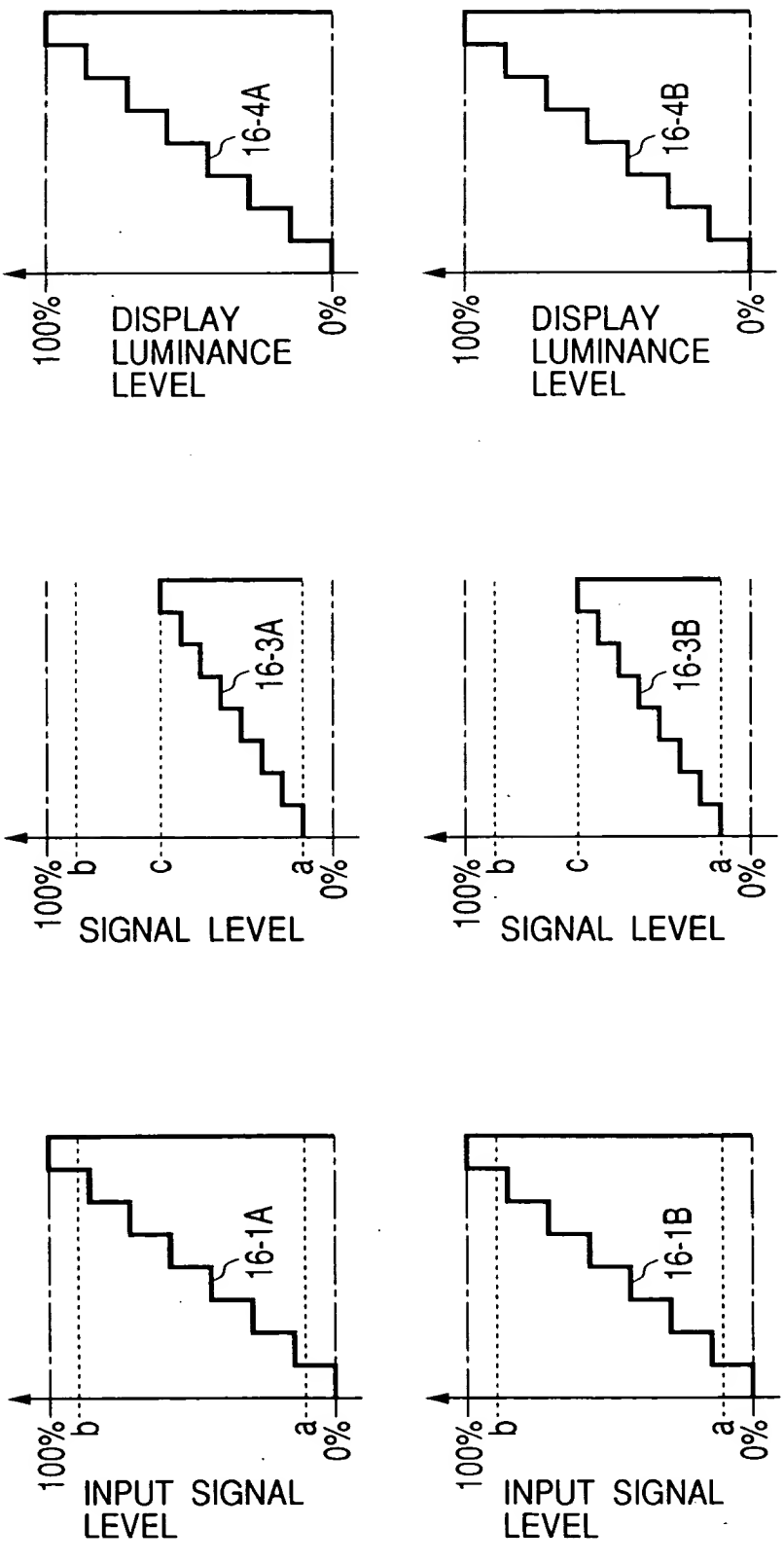
16-4A
100%
DISPLAY LUMINANCE LEVEL
0%
16-4B
100%
DISPLAY LUMINANCE LEVEL
0%
16-3A
100%
b
c
a
0%
SIGNAL LEVEL
16-3B
100%
b
c
a
0%
SIGNAL LEVEL
16-1A
100%
b
a
0%
INPUT SIGNAL LEVEL
16-1B
100%
b
a
0%
INPUT SIGNAL LEVEL

FIG. 30

FIG. 30A	FIG. 30B

FIG. 30A

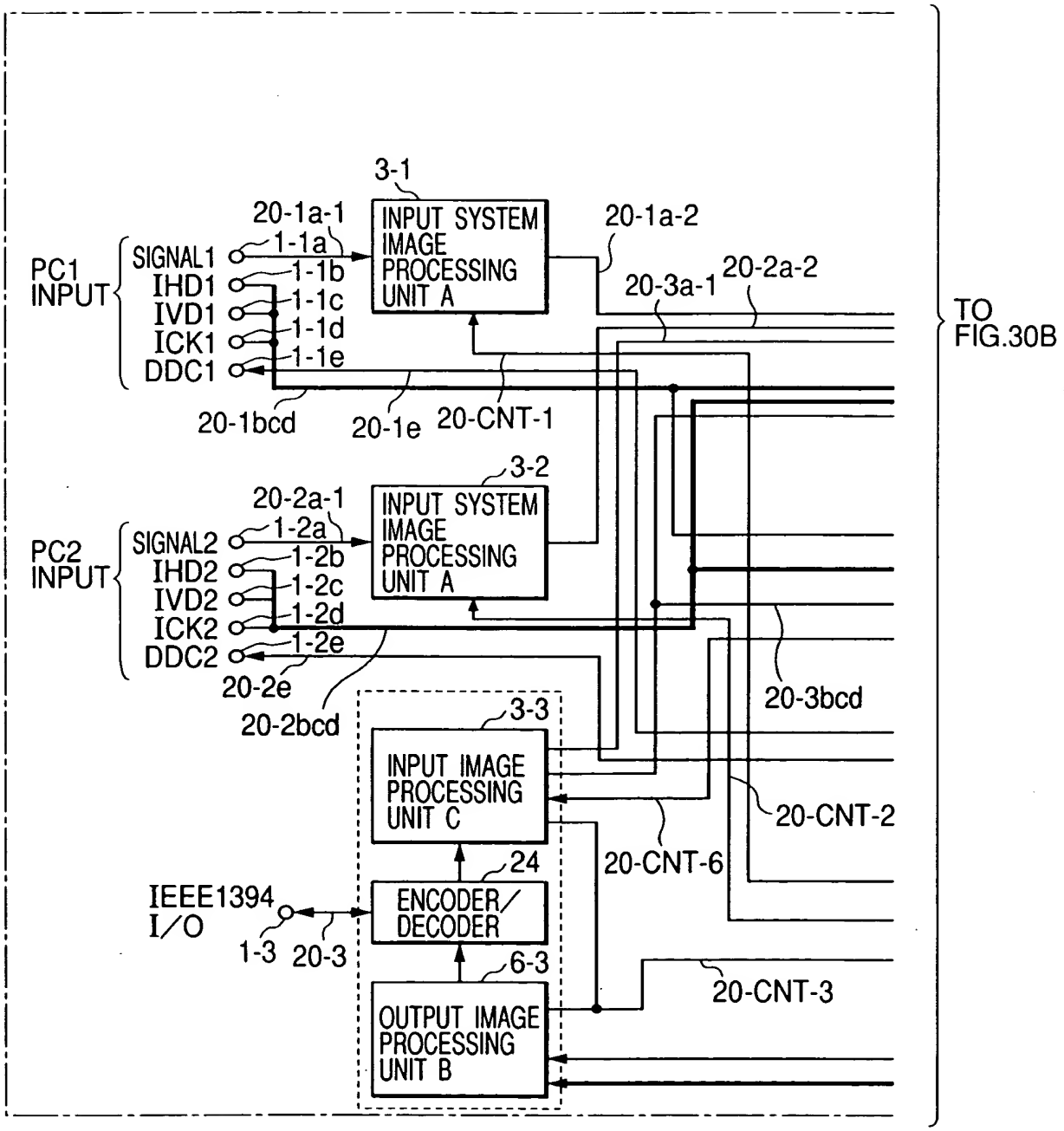

FIG. 30B

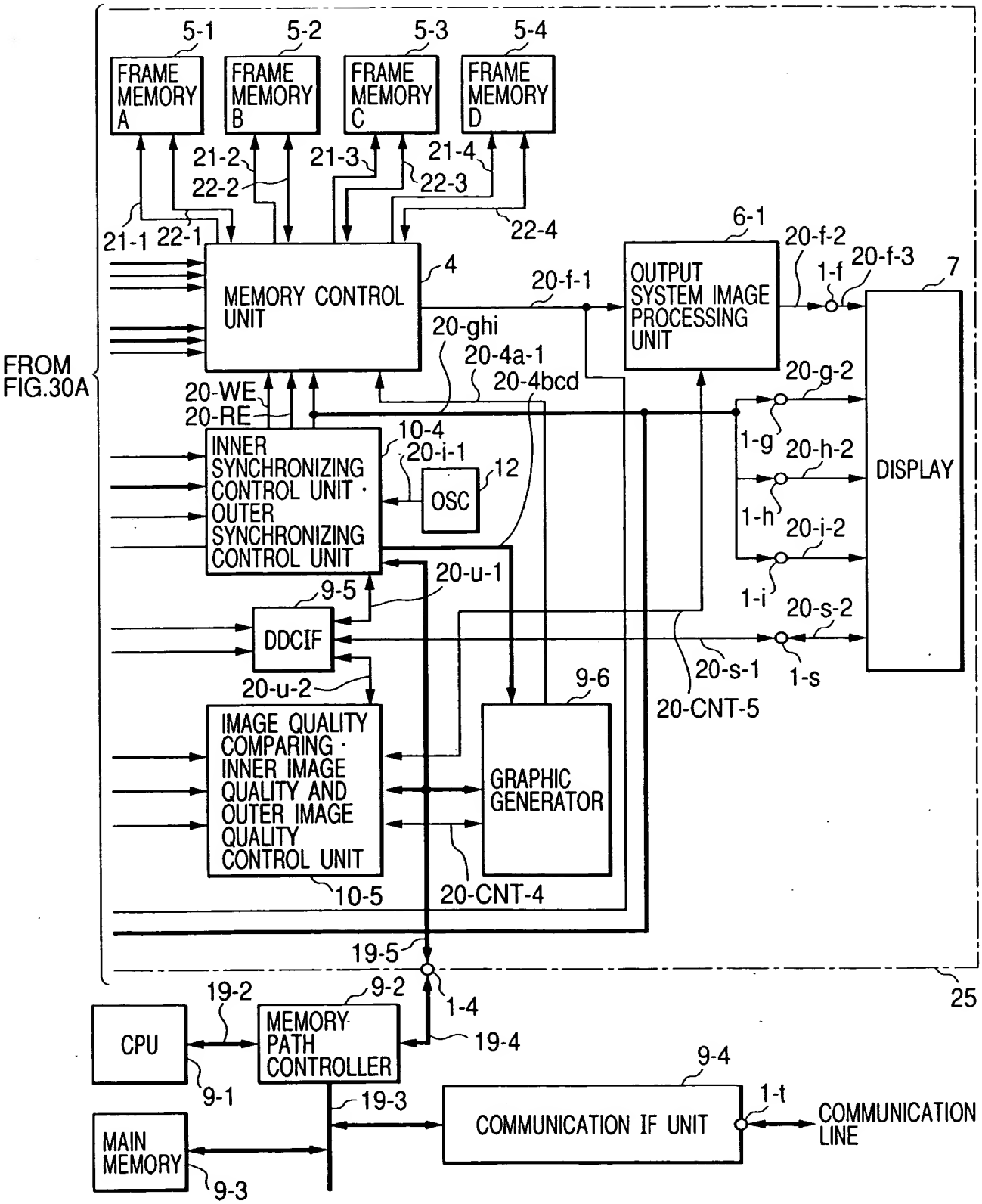
FROM FIG.30A
5-1
FRAME MEMORY A
5-2
FRAME MEMORY B
5-3
FRAME MEMORY C
5-4
FRAME MEMORY D
21-1
22-1
21-2
22-2
21-3
22-3
21-4
22-4
MEMORY CONTROL UNIT
4
20-f-1
6-1
OUTPUT SYSTEM IMAGE PROCESSING UNIT
20-f-2
1-f
20-f-3
7
20-ghi
20-4a-1
20-4bcd
20-WE
20-RE
20-g-2
1-g
20-h-2
DISPLAY
10-4
INNER SYNCHRONIZING CONTROL UNIT · OUTER SYNCHRONIZING CONTROL UNIT
20-i-1
OSC
12
1-h
20-i-2
1-i
20-s-2
20-u-1
9-5
DDCIF
20-s-1
1-s
20-CNT-5
20-u-2
9-6
IMAGE QUALITY COMPARING · INNER IMAGE QUALITY AND OUTER IMAGE QUALITY CONTROL UNIT
GRAPHIC GENERATOR
10-5
20-CNT-4
19-5
25
19-2
9-2
1-4
CPU
MEMORY PATH CONTROLLER
19-4
9-1
19-3
9-4
1-t
COMMUNICATION IF UNIT
COMMUNICATION LINE
MAIN MEMORY
9-3

FIG. 31A

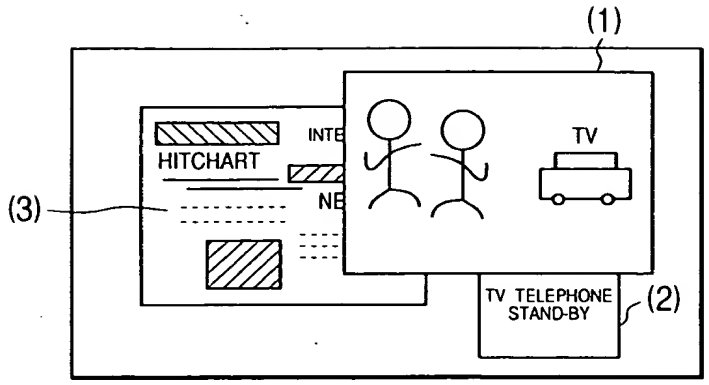

FIG. 31B

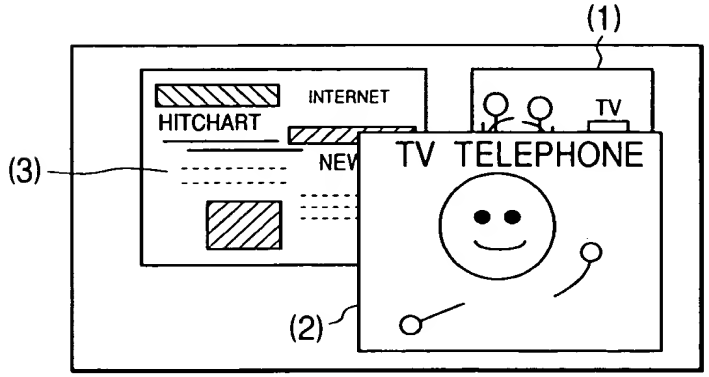

FIG. 31C

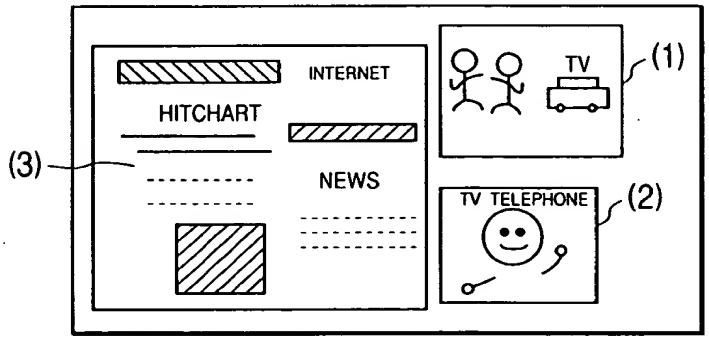
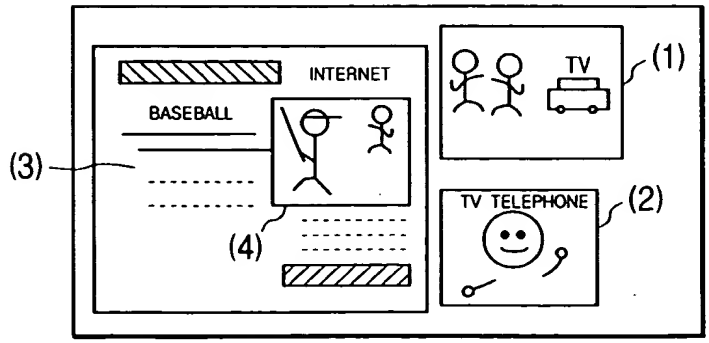
FIG. 31D